A STUDY OF PULSE - WIDTH CONTROLLED AC - DC CONVERTER FED DC MOTOR

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By

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CERTIFICATE

This is to certify that the work on "A STUDY OF PULSE-WIDTH CONTROLLED AC/DC CONVERTER FED DC MOTOR" by P.D. Parikh has been carried out under my supervision and this has not been submitted elsewhere for a degree.

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P.D. Parikh

TABLE OF CONTENTS

Page

LIST OF PRINCIPAL SYMBOLS

E_m	maximum supply line voltage, volts
w	angular frequency of line voltage, rad/sec.
i_S	supply line current, amps.
m	modulation index
p	number of pulses
k	pulse number
t	time, secs.
d	pulse width
α	firing angle
β	extinction angle
v_d	converter output dc voltage, volts
v_{dm}	converter output maximum voltage, volts
i_d	converter output current, amps
ω_s	speed of motor, rad/sec.
N	speed of motor, rpm
a_1, b_1, a_2	fourier coefficients
Q_L	load quality factor $= \omega L_A / R_A$
φ	load phase angle, radians
E	back emf of motor, volts.
R_A	eddy current model motor armature resistance
L_A	eddy current model motor armature inductance
V_C	voltage across capacitor, volts
i_{L_1}	current in inductance L_1, amps.
i_{L_2}	current in inductance L_2, amps.

i_{D_2}	current through diode D_2, amps.
$Z_1, Z_2, \ldots Z_5$	state variables
V_D	drop across thyristor, volts
V_S	drop across thyristor, volts
i_C	capacitor current, amps.

LIST OF FIGURES

ABSTRACT

In this thesis, a simple and versatile ac-dc converter employing forced commutation is analysed with both R-L and separately excited dc motor loads. The analysis of such a converter with a motor load is lacking in literature. Equal pulse width modulation with five pulses per half cycle of supply voltage is adopted. Generalized state equations are derived for the converter circuit, modelling the switching devices by binary logic modules. The modes of operation of the converter circuit and their sequence need not be known apriori. These are obtained by digital simulation.

The speed-torque characteristics of a separately excited dc motor with equal pulse width modulation are obtained and compared with those obtainable from a phase controlled converter showing the boundary between continuous and discontinuous conduction regions. The study reveals significant improvements with pulse-width controlled ac-dc converter.

A novel firing circuit which is suitable for both rectifier and inverter operations is developed for implementing equal pulse width modulation. The firing strategy does not require commutating capacitor precharging while starting the converter initially. Experimental verification shows that there is complete agreement between digital simulation and experimental results, with regard to modes of operation of converter circuit, speed-torque characteristics and supply power factor.

CHAPTER I

INTRODUCTION

With the advent of high power semiconductor switches and low power IC technology, solid state speed control of a dc motor is playing an important role in the variable speed industrial drive systems. Unlike an ac motor, a dc motor is basically a variable speed motor,with versatile speed-torque characteristics. The dc motor is therefore the most commonly used drive motor in industrial drive system where variable speed operation is required. The control module for a dc motor is relatively simple and less expensive.

Thyristor converters are used for converting ac to dc. Phase delay control is commonly used in the thyristor converters to obtain variable dc voltage. These converters with phase delay control suffer from the serious drawbacks of poor displacement factor with increasing phase angle delays. Harmonic currents are generated in the ac supply line. As a result, the supply power factor deteriorates considerably with increasing phase angle delays. Ripple is also produced in the output current. The output current may also become discontinuous. Filter chokes are inserted in the output of a thyristor converter in order to reduce ripple in the output current and eliminate discontinuous conduction (if any). The use of filter chokes is not desirable as this may result in low efficiency, high cost and poor time response.

Half-controlled converters, converters with astmmetrical control and sequence control [1] have come into existence specifically with a view to improve power factor. Phase delay control is still used in such converters and the displacement factor is not very much improved.

It is possible to keep the displacement factor or fundamental power factor at unity if the supply voltage is switched symmetrically with respect to the peak of the supply voltage. Such a control technique is termed as 'pulse width modulation'. Since the supply voltage is to be disconnected before the voltage reverses, ac line commutation is not possible. In recent years, a new class of forced commutated thyristor converters emerged [2]. The modulation technique which is an alternative to phase control technique was selected based on selective input harmonic elimination [3],maximum supply power factor[4]and continuous armature current conduction [4]. The converters used by different researchers were relatively complex. They are mostly suitable for rectification mode. However, a simple and versatile converter circuit was suggested by Kataoka [5]. The converter was analysed with only RL load to a limited extent.

In this thesis, the simple and versatile thyristor converter circuit suggested by Katoaka has been taken up for a detailed investigation with both RL load and a separately excited dc motor load. Pulse-width modulation with several switching in each half cycle of supply voltage is considered. The supply displacement factor, distortion factor, power factor, supply current harmonics and output current continuous and discontinuous regions are investigated for the pulse-width modulation. Section 1.1 deals with the content of the thesis chapter wise.

1.1 OUTLINE OF THESIS

Chapter II deals with the various power circuits for the implementation of pulse-width control scheme. The operation

of each circuit is described. Also the limitations of each circuit are pointed out. Finally a power circuit which is simple and versatile has been selected for a detailed investigation.

Abrol [6] has compared the modulation schemes on the basis of their external performances with R-L load. As the equal pulse-width modulation has the maximum voltage variation range, the other performances being quite comparable with those obtainable from other modulation schemes, this particular modulation scheme is adopted. Modulation schemes for which the maximum output voltage is less than the maximum possible voltage ($2 E_m/\pi$) require a power transformer on the input side to achieve a speed control which is comparable to a modulation scheme having an output voltage range from 0 percent to 100 percent. This increases the cost factor.

Chapter III deals with equal pulse-width modulation for analysing the output voltage variation. Also the input line current has been analysed for a motor load using the actual current waveform. The boundary between continuous and discontinuous conduction for five pulses in each half cycle has been obtained and plotted on a normalized speed -torque plane. For the sake of comparison, the boundary for the half-controlled converter with phase delay control is also given. The minimum inductance estimation for a given speed-torque characteristic for continuous conduction is explained. Operating diagram [7]

is developed for pulse-width modulated converter, supplying general load circuit parameters. Also minimum inductance calculation for continuous conduction with load circuit parameters is presented.

The analysis of a particular converter selected on the basis of studies presented in Chapter II, is dealt with in Chapter IV with motor and R-L load. Equal pulse-width modulation is adopted in analysing the converter circuit digitally. The binary logic modules are used for representing the devices. The method of simulation does not require apriori knowledge of sequence of modes of operation of the converter circuit. The speed-torque characteristics are also obtained taking the commutation effect into account. The effect of LC resonant time of the commutation circuit on the torque-speed characteristics is investigated. Turn-off characteristics of SCR's S_1 and S_2 are also investigated.

A novel firing circuit which can be used for rectification and regenerative operation(with slight modification in logic)is developed in Chapter V. The firing circuit has the self starting property (no necessity of precharging the commutating capacitor). The operation of the converter circuit is studied experimentally. The torque-speed characteristics and input line power factor (predicted theoretically earlier)are verified experimentally. Also, some of the steady-state waveforms

obtained by digital simulation are verified experimentally. There has been a good agreement between experimental and simulation results.

Lastly, conclusions are drawn and recommendation for further work are given in Chapter VI.

CHAPTER II

AC-DC CONVERTER CIRCUITS USING FORCED COMMUTATION

2.1 INTRODUCTION

Phase controlled converters have an inherent drawback of decreasing displacement factor as the firing angle is increased, thus drawing large lagging reactive power corresponding to the fundamental current from the source. Since the supply current is non-sinusoidal, harmonics are also generated in the input ac lines. The supply harmonic currents produce communication interference, transmission losses, relay and equipment malfunctioning [8].

As a consequence of the above, a number of schemes were developed to improve upon the shortcomings. Most of the initial schemes involved line commutation, e.g. assymmetrical control[9]use of freewheeling action[10], Sequence control[9]. With the availability of high quality inverter grade SCR's, forced commutation schemes using pulse width control became prominent. The main advantage of pulse width controlled forced commutated converters is that the fundamental power factor remains unity irrespective of the output voltage. Also the frequency spectrum of supply current is shifted from the predominant lower order harmonics to

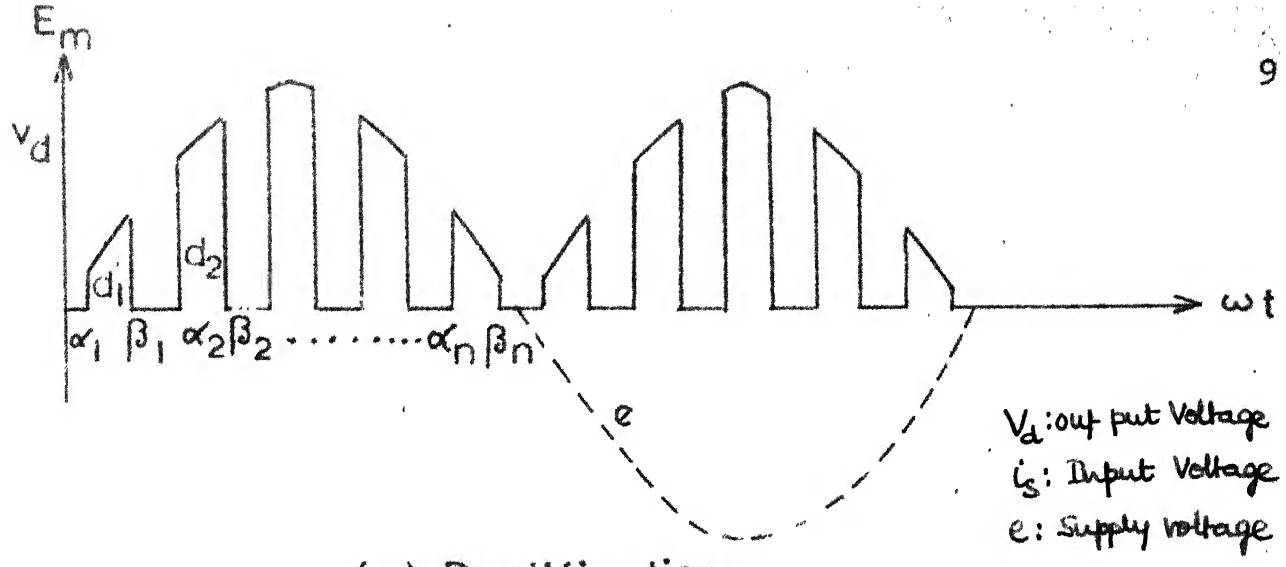
higher order harmonics by a judicious choice of pulse-width control scheme. The higher order harmonics can be easily filtered out using inexpensive filters.

The basic principle of pulse width control is shown in Fig. 2.1. The main thyristors of the converter that are conducting are turned off once or several times in each half cycle of the A.C. line voltage to obtain a pulse shaped output voltage. The mean output voltage is varied by varying the pulse widths d_1, d_2 etc. Since the pulses are symmetrical about a quarter cycle, varying d_1,d_2, ..., does not introduce a phase lag in the input line current.

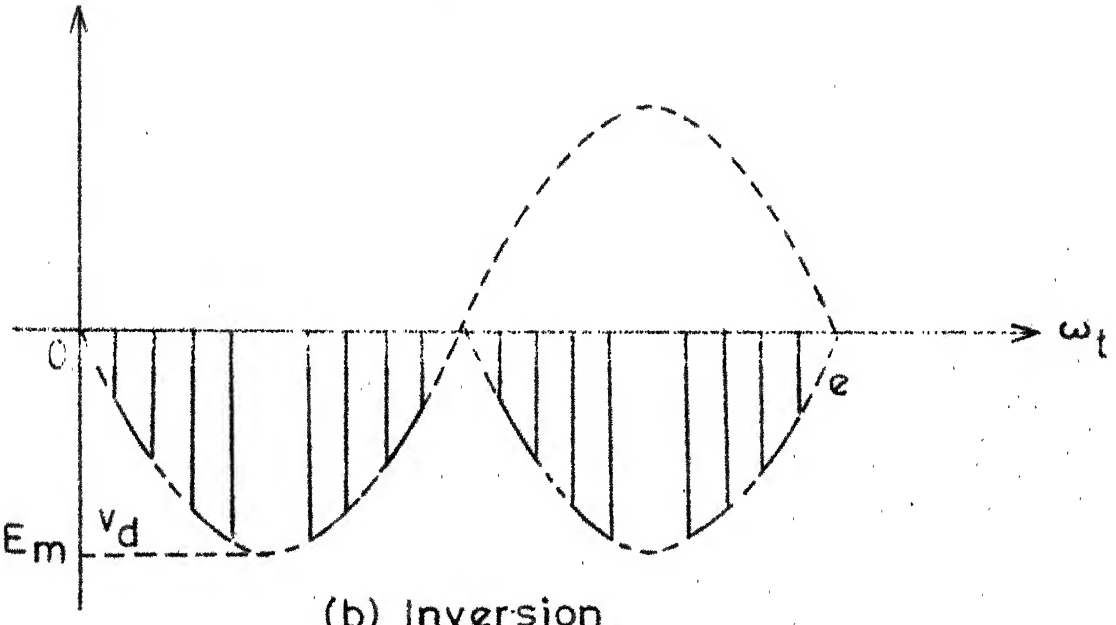
For the implementation of the pulse width control scheme a power circuit is required. In this chapter the different power circuits have been discussed based on the type of commutation used. The operation of each power circuit is explained and the limitations pointed out. Finally, a particular power circuit which is simple and versatile has been selected for implementing the forced commutation scheme.

2.2 AC-DC CONVERTER USING DIODE RECTIFIER AND CHOPPER

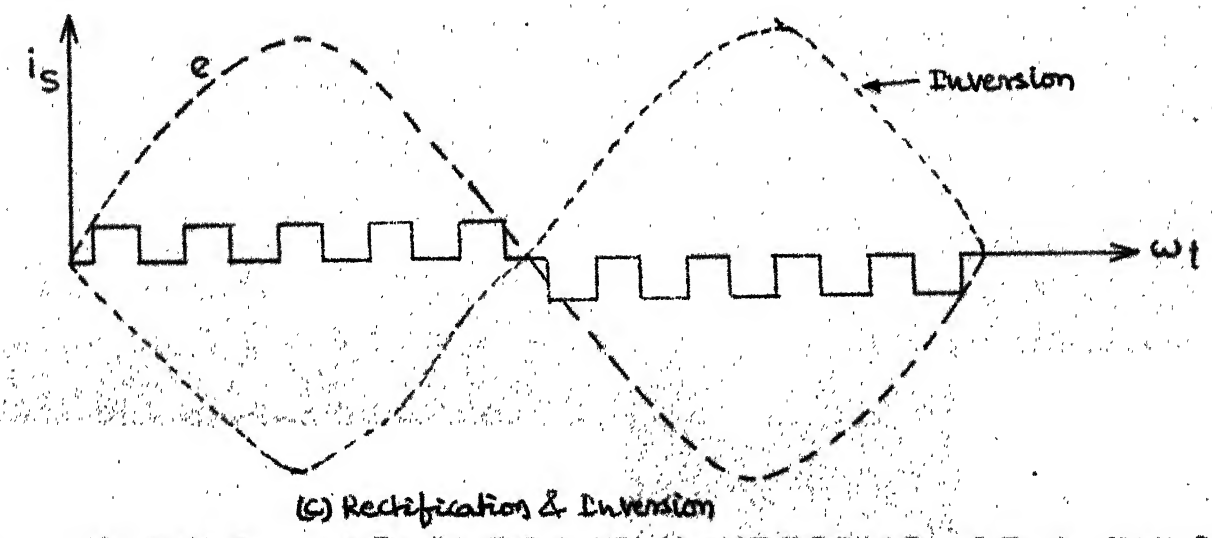
Figure 2.2 shows the circuit configuration for the converter. It consists of an uncontrolled converter bridge followed by a DC chopper. The D.C. chopper can be one of the many chopper configurations. It may be operated with auxiliary type or complimentary type of commutation. The chopper can be



(a) Rectification



(b) Inversion



(c) Rectification & Inversion

IG. 2.1 VOLTAGE AND CURRENT WAVEFORMS OF A PULSE-WIDT CONTROL AC TO DC CONVERTER FOR RECTIFICATION A INVERSION

switched ON and OFF a number of times to get the pulse type voltage waveform of Fig. 2.1. The output voltage can be varied by controlling the ON and OFF times of the chopper.

The converter circuit of Fig. 2.2 cannot be used in the inversion mode since the output voltage is always positive. The circuit is inherently inefficient because of additional losses in the diode bridge. The output voltage variation range is dependent on the type of chopper used and the commutation phenomena utilized.

2.3 SINGLE PHASE AC-DC CONVERTER USING AUXILIARY COMMUTATION

2.3.1 Circuit-1

The circuit configuration is shown in Fig. 2.3.1 [11]. The two inverse parallel connected SCRs (S_1 and S_2) are the main SCR's. SA_1 and SA_2 are the auxilliary SCRs used to commutate the main SCRs. Capacitors C_1 and C_2 are the commutating capacitors which are initially charged through D_1 and D_2 to E_m with polarities as shown. D_3, D_4, D_5 and D_6 form the uncontrolled bridge. When line b is positive S_1 is fired, connecting the line voltage through the uncontrolled bridge to load. When it has to be turned OFF the auxilliary SCR SA_1 is turned ON connecting capacitor C_1 directly across S_1, which thus turns OFF. The load current freewheels through the uncontrolled bridge. The charging of C_1 with reverse polarity starts taking place through SA_1 and load and it follows the

supply voltage. During the negative half cycle S_2, SA_2 and C_2 come into operation.

The main drawback of this circuit is that the circuit complexity increases for larger number of output voltage pulses. The circuit as such illustrated in Fig. 2.3.1 is suitable for one pulse of voltage in each half cycle. Each additional pulse per half cycle requires two diodes, two thyristors and two capacitors in the circuit making the circuit highly uneconomical. Also it cannot support regeneration.

2.3.2 Circuit-2

The circuit configuration is shown in Fig. 2.3.2a [1]. The circuit utilizes external auxiliary voltage pulse commutation. The circuit is a combination of an ac chopper (connection of S_1 and S_2 in inverse parallel) and an uncontrolled bridge converter (D_1,D_2,D_3,D_4). TS_1 and TS_2 are the secondaries of the transformer which is used for commutating SCR S_1 and S_2 respectively. Fig. 2.3.2b forms the auxilliary commutation circuit.

When 'a' goes positive S_1 and S_3 are both fired simultaneously. The commutating capacitor C starts charging due to the resonant path formed by V_{DC}, L_1,S_3 and C to the polarity shown. At the same time the line voltage is connected to the load. When turn-off of S_1 is required, SCR S_4 of the commutation circuit is fired. The whole of the capacitor voltage appears in the

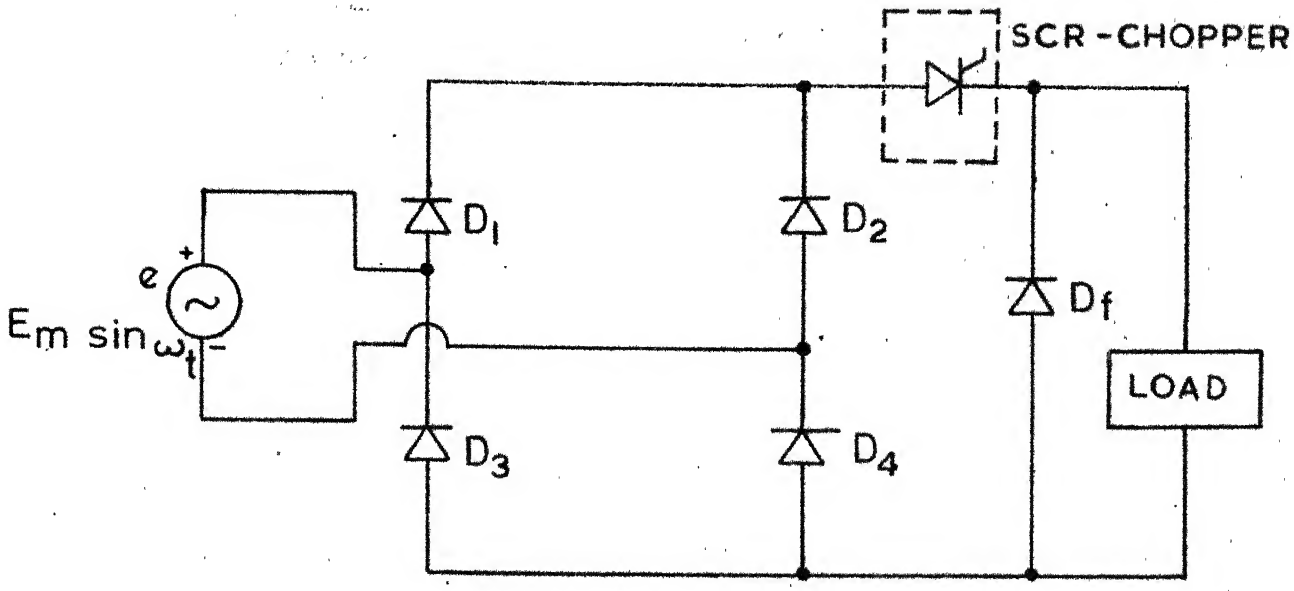


FIG. 2.2 SINGLE PHASE AC-DC CONVERTER

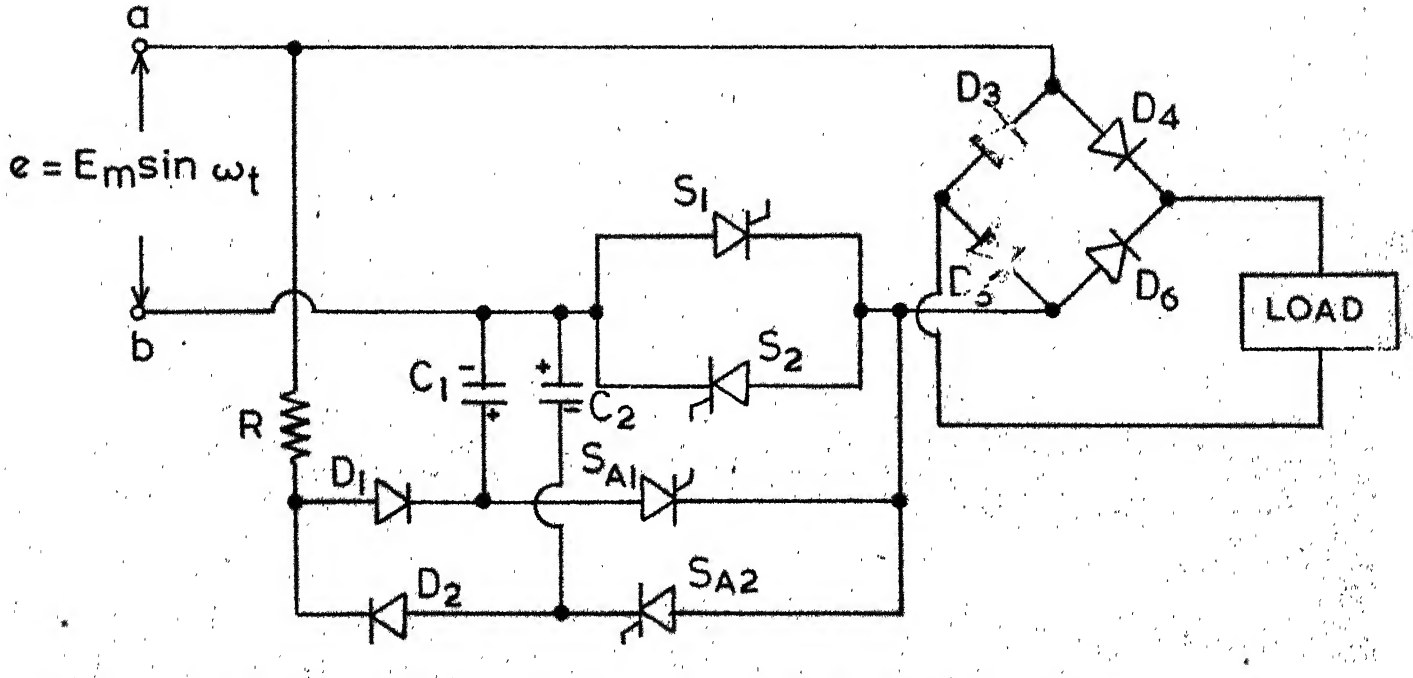


FIG. 2.3.1. SINGLE PHASE AC-DC CONVERTER USING AUXILIARY VOLTAGE COMMUTATION

secondary TS_1 which reverse biases S_1 and turns it OFF. Capacitor C discharges through the primary TP and changes polarity of charge. Capacitor C_1 is provided for limiting the forward dv/dt rating of SCRs S_1 and S_2.

When'a'goes negative, S_2 serves as the main thyristor while S_3 and S_4 serve the same function.

This circuit is an improvement upon the previous circuit in that it can support larger number of pulses with no additional requirement of elements.

Requirement of an auxilliary dc supply and a transformer increases the cost and also the circuit cannot support regeneration.

2.3.3 Circuit-3

Another circuit which utilizes auxilliary current commutation is shown in Fig. 2.3.3a[12].SCRs S_1,S_2,S_3 and S_4 form the main thyristors. S_5 is the auxilliary thyristor used to turn-off SCRs S_1 or S_2. Similarly S_6 is the auxilliary thyristor used to turn-off SCRs S_3 or S_4. Diodes D_1 to D_4,capacitances C_1 and C_2, inductances L_1 and L_2 are used as commutating elements. S_1 and S_4 are turned ON when source voltage is positive. S_2 and S_3 are turned ON when source voltage is negative. A large inductive load has been assumed to simplify analysis.

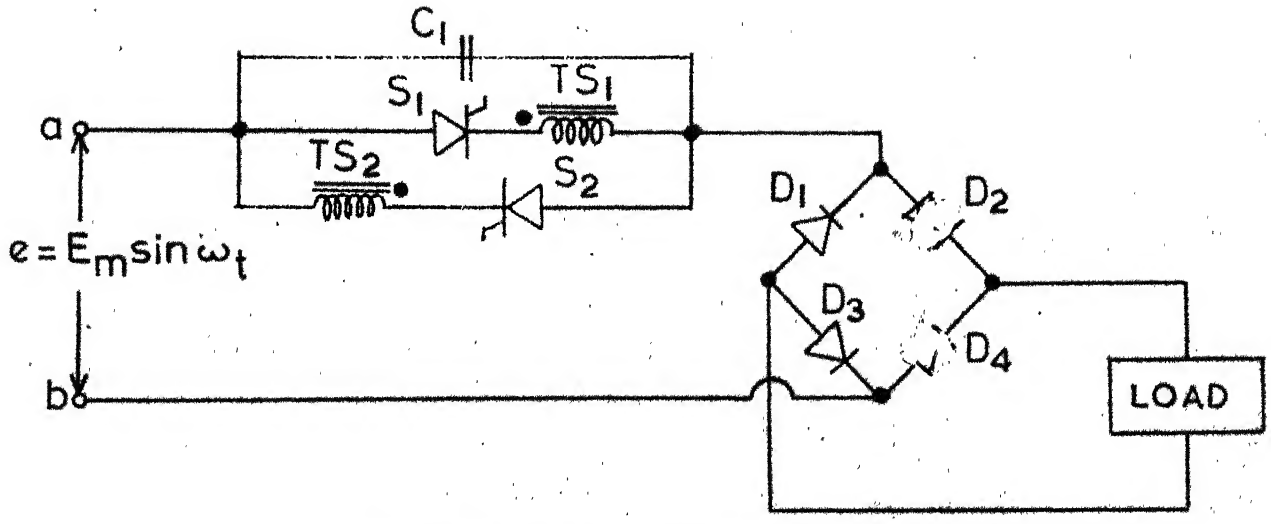


FIG. 2.3.2a. POWER CIRCUIT

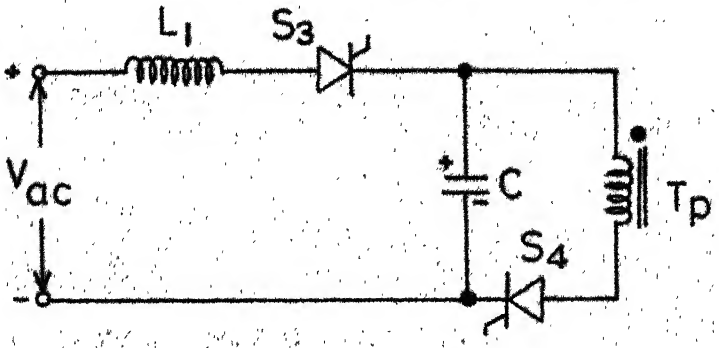


FIG. 2.3.2b COMMUTATION CIRCUIT

Suppose source voltage is positive and SCRs S_1 and S_4 are conducting, thus power is fed to the load. The various transients which occur when transfer from S_4 to S_3 is done are shown in Fig. 2.3.3b. S_6 is gated, current (i_1) starts flowing through it and the polarity of charge on capacitor C_2 changes after half the cycle of L_2-C_2 resonant period. The current i_1 goes to zero at the end of half cycle (time t_1), turning S_6 OFF. D_4 now becomes forward biased and hence starts conducting and the current i_2 starts flowing through it. Current builds up in the resonant circuit L_2-C_2-D_4-S_4 and when it becomes equal to the load current I_L, S_4 stops conducting (time t_2). As soon as S_4 stops conducting, the current $i_3 = I_L$ starts flowing through C_2-L_2-D_4-e charging again C_2 linearly with a positive charge. S_4 will be reverse biased till capacitor voltage becomes zero. At time t_3 capacitor voltage becomes greater than e and S_3 is forward biased and will be turned ON as soon as it is gated. Load current I_L starts flowing in the path S_1 - load - S_3 thus disconnecting the load from supply.

Now when the supply voltage e is greater than zero, S_4 will remain forward biased. Say S_1 and S_3 are conducting and now if S_4 is gated it will turn ON and the load current will be transferred from S_3 to S_4.

When the source e is negative, the SCR's S_2 and S_3 allow the transfer of power to the load from the source. When switching has to be done to S_4 from S_3 (freewheeling), the same modes occur as that when switching was done from S_4 to S_3 and e was greater than zero. Since S_3 remains forward biased, (e is negative) when it is triggered the load current shifts from S_4 to S_3 with S_4 turning OFF.

D_1, D_2, S_5, C_1 and L_1 come into picture when switching from S_1 to S_2 and vice versa is required.

The above circuit can also work in the regenerative mode. In this case, S_3 and S_2 are turned ON during the positive half cycle while S_1 and S_4 are turned ON during the negative half cycle.

The commutation circuit is rather complex requiring a large number of components. Another disadvantage of the circuit is that the DC output voltage variation will be limited both on the lower side and the higher side. Fig. 2.3.3b shows the waveform during the commutation transient when S_3 takes over from S_4. Before S_3 conducts, the auxilliary thyristor S_6 is triggered giving a pulse of current of duration t_1 secs. The presence of such a pulse of current whenever a main thyristor is to be turned OFF, imposes a restriction on the output voltage variation. S_3 can be fired only when the capacitor voltage becomes greater than input line voltage

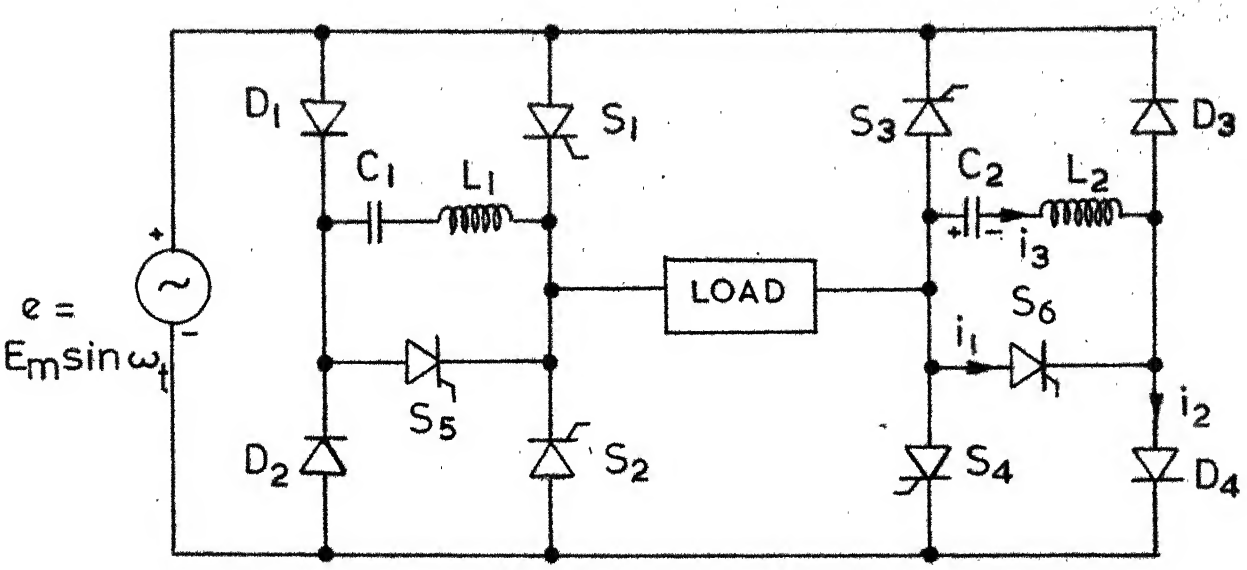


FIG. 2.3.3a. SINGLE PHASE AC-DC CONVERTER USING AUXILIARY CURRENT COMMUTATION

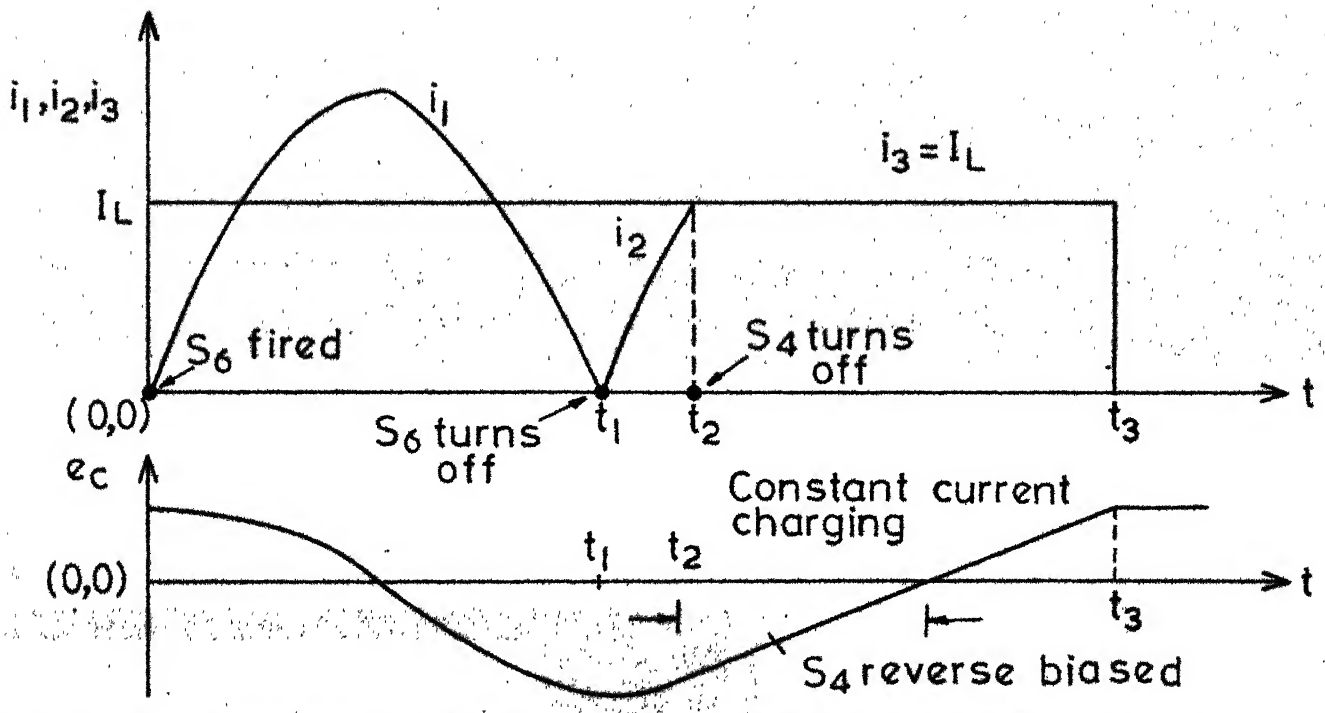


FIG. 2.3.3b. CURRENT AND VOLTAGE TRANSIENTS DURING COMMUTATION

at time t_3. This imposes a further restriction on the output voltage variation.

2.3.4 Circuit-4

Another circuit which uses auxilliary commutation [13] is shown in Fig. 2.3.4. S_1 and S_2 are the main thyristors while S_3 and S_4 are the auxilliary thyristors used to turn-off S_1 and S_2 respectively. C_1 and C_2 are the commutating capacitors, charged initially to E_m in the direction shown, diodes D_1 and D_2 are the main diodes, while D_3 and D_4 are diodes which allow charging of capacitors C_1 and C_2 respectively.

When the supply voltage e is positive with the polarity shown in Fig. 2.3.4, S_1 and D_2 are forward biased and if S_1 is gated, it will turn-on connecting the source voltage across the load circuit, thus delivering power from the ac source to the load circuit during the positive half-cycle.. D_2 helps charging up of capacitor C_2 in the direction shown. Whenever S_1 is to be turned OFF S_3 is fired applying full capacitor voltage across S_1 and thus turning it OFF. The capacitor C_1 starts charging with the load current in the opposite direction, through the path e-C_1-S_3-load-D_2-e. When the capacitor voltage reverses and becomes equal to the line voltage, the diode D_1 conducts and the load current freewheels through the diodes D_1 and D_2. The thyristor S_3 turns OFF as it is reverse biased by two diode drops ($V_{D_1} + V_{D_2}$). During the other

half cycle C_1 charges back to E_m in the original direction through D_3. The circuit is suitable for only one output pulse of voltage per half cycle. The converter circuit requires two commutating capacitors and is fairly complex. Also it cannot be used in the inversion mode.

2.4 SINGLE PHASE AC-DC CONVERTER USING EXTERNAL PULSE COMMUTATION

The circuit diagram is shown in Fig. 2.4 [6.]. A pulse forming network (PFN) is utilized for commutation purposes. The principle behind external pulse commutation is that, if a commutation pulse of amplitude greater than the load voltage and duration greater than the turn-off time of SCRs is applied at the converter output terminals, the conducting SCRs turn OFF.

Referring to Fig. 2.4, the SCRs S_1 and S_2 are the main SCRs while S_a, S_b and S_c are the auxilliary SCRs which together with PFN and ausilliary supply E_a form the commutation network. D_F is the freewheel diode which provides a path for the load current (inductive load) when the main SCRs are OFF. When a is positive, S_1 and S_a are gated simultaneously. Power is fed to the load and simultaneously the PFN starts charging from the auxilliary supply E_a. The SCR S_a stops conduction when the PFN is fully charged up. When the SCR S_1 is to be turned OFF, the SCR S_b is fired which

reverse biases S_1 and turns it OFF. The load current is supplied by the PFN through the SCR S_b. This reverse bias is maintained for enough time such that the SCR which was conducting earlier is commutated and regains its forward blocking capacity. To complete the commutation process the SCR S_c is fired. This enables the PFN to discharge through it and the load current freewheels through the diode D_f.

For the regenerative operation, the converter circuit is to be modified slightly. The diode D_f has to be replaced by the SCR S_F. Also a smoothing reactor is required. The SCR S_F is fired such that the load current freewheels through the circuit formed by S_F, load and smoothing reactor. The SCR S_F is turned OFF in the same way as the main SCRs were turned OFF in the rectification mode. After the PFN is discharged through S_c, the main SCR having negative voltage across it is gated. Because the current is falling in the smoothing reactor, the voltage across it adds to the emf of the load and becomes greater than the instantaneous input voltage. The gated main SCR becomes forward biased and starts conducting and energy is fed back to the supply. With subsequent firing of S_f, load current starts freewheeling and the conducting main SCR turns OFF as its anode voltage is negative.

The scheme suffers from the following drawbacks :

The auxilliary thyristors are required to have high di/dt and voltage ratings. The same circuit cannot be used

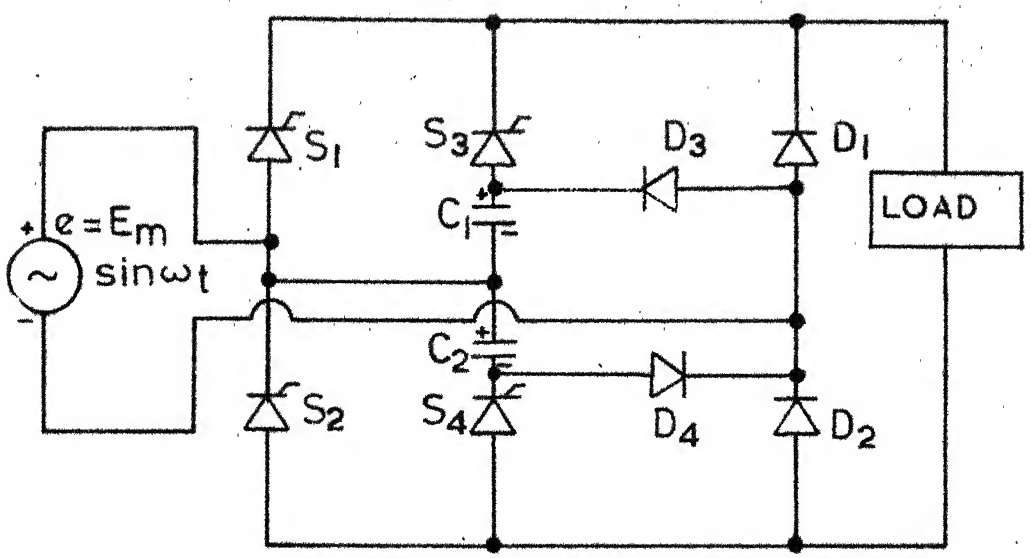


FIG. 2.3.4. SINGLE PHASE AC-DC CONVERTER USING AUXILIARY VOLTAGE COMMUTATION

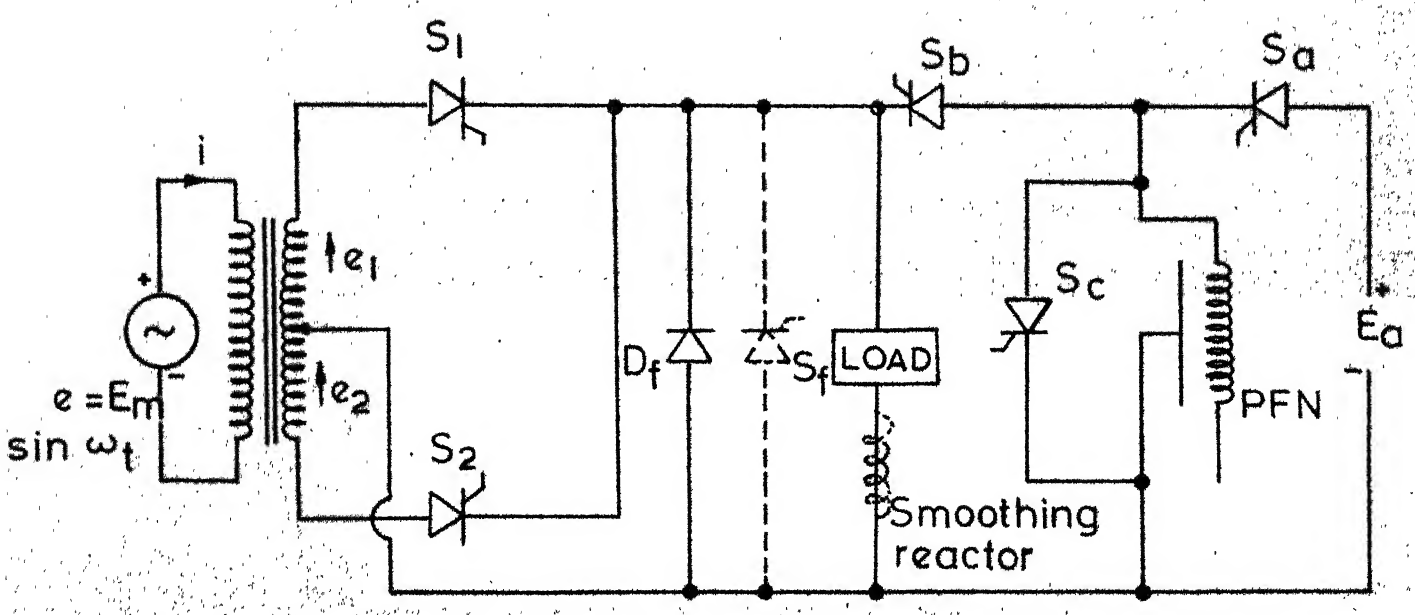


FIG. 2.4 SINGLE PHASE AC-DC CONVERTER USING EXTERNAL PULSE COMMUTATION

for rectification and inversion. Auxilliary thyristors are required, increasing the complexity. Also an auxilliary dc supply is required. Another drawback is the limitation imposed on the range of output voltage by the charging time and the discharging time of the PFN, for until the PFN charges up the main SCR conducting cannot be turned OFF (rectification) and similarly the main SCR cannot be turned ON until PFN discharges through S_c.

2.5 SINGLE PHASE AC-DC CONVERTER USING COMPLEMENTARY COMMUTATION

The circuit diagram is shown in Fig. 2.5 [5]. The SCR's S_1 and S_2 are turned ON and OFF several times in each cycle of the supply voltage and therefore these must be of inverter grade with low turn-off time. The SCRs S_3 and S_4 are ac line commutated and hence they can be of converter grade. The SCRs S_1 to S_4 form the conventional single phase bridge. The capacitor C and inductances L_1 and L_2 are the commutating elements used for commutating the SCR's S_1 and S_2. Diodes, D_1, D_2, D_{L_1} and D_{L_2} prevent the capacitor from loosing its charge which is essential for commutation. L_s is the source inductance inserted to overcharge the capacitor ($I_{load}\sqrt{(L_s/C)}$) for better commutation especially when the supply voltage is low.

Assume that the capacitor C is charged in the direction shown in Fig. 2.5. When the line voltage is positive S_1, D_1 and S_4 conduct to feed power to the load. When S_1 is to be turned OFF, S_2 is fired applying full capacitor voltage across S_1 and thus turning it OFF. The capacitor starts charging up in the other direction by two paths, one through the load current and the other through the loop formed by S_2-D_{L_1}-L_1-C-S_2. The second path formed by the loop makes the charging independent of load. When the capacitor voltage becomes equal to the line voltage, the diode D_2 starts conducting. Because of the presence of L_s, D_1 continues to conduct but current through it goes on decreasing while current in D_2 builds up gradually to load current. When current in D_1 falls to zero, then load current freewheels through S_2, D_2 and S_4.

When S_1 is triggered again, S_2 goes OFF. Capacitor C starts charging up and when it becomes equal to the line voltage, D_1 starts conducting. Due to the presence of the inductor L_s in the supply line, the transfer of current from D_2 to D_1 is gradual. The load current through S_4,D_2,C and S_1 decreases gradually to zero while the current through the source e, D_1,S_1, load and S_4 steadily increases to full value. At this instant, D_2 turns OFF and the load current is supplied by the ac voltage, thus transferring power to the load circuit.

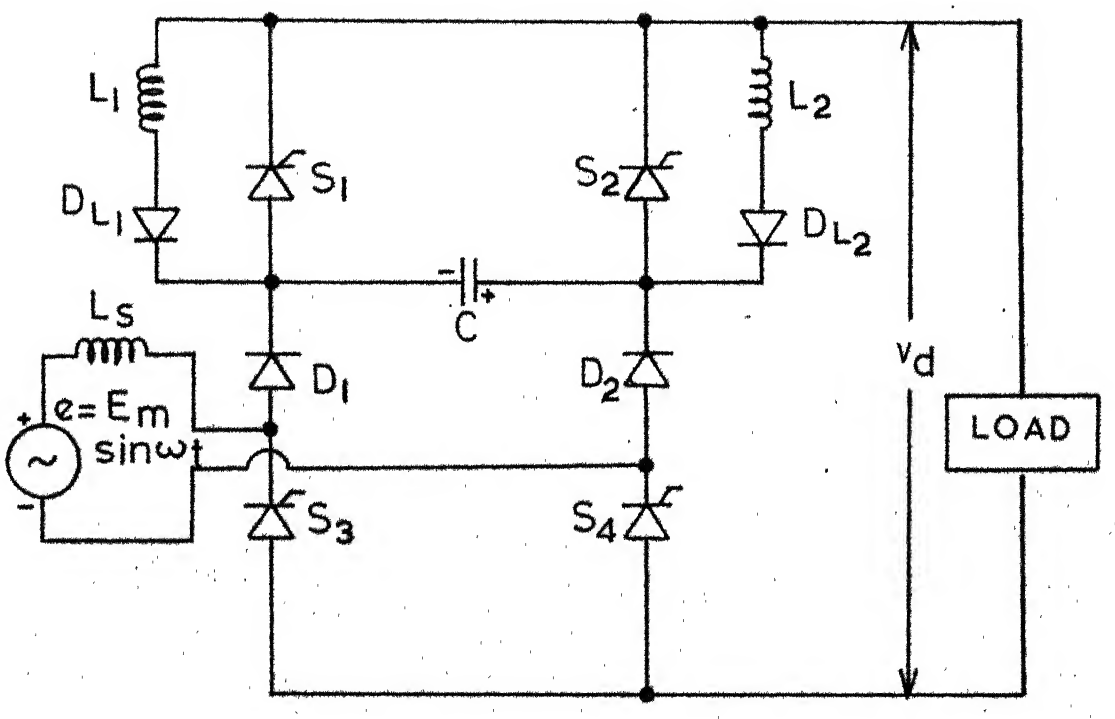


FIG.2.5 SINGLE PHASE AC-DC CHOPPER USING COMPLIMENTAR COMMUTATION

The same circuit can be used for inversion mode also by applying trigger pulses to (S_1 and S_4) and (S_2 and S_3) in the negative and positive half cycles of supply voltage.

This is a simple converter circuit requiring a minimum number of components. Both rectification and inversion operations are possible with the same power circuit. No additional dc power supply is required. Single as well as multi-pulse width control can be easily implemented with this converter circuit.

2.6 CONCLUSIONS

All the circuits discussed in Sections 2.2 to 2.4 suffer from one of the following disadvantages. Most of them have complex commutation circuits requiring auxilliary SCRs having higher voltage and current ratings. Some of them require auxilliary dc power supplies, thereby increasing the power requirements and increasing cost. Most of the circuits do not have the regeneration capability or can regenerate only with modifications in their basic structure. Some circuits have load dependent commutation, also for some of them some minimum time has to be provided before commutation could be achieved. These facts restrict the output voltage variation range on both lower as well as higher sides.

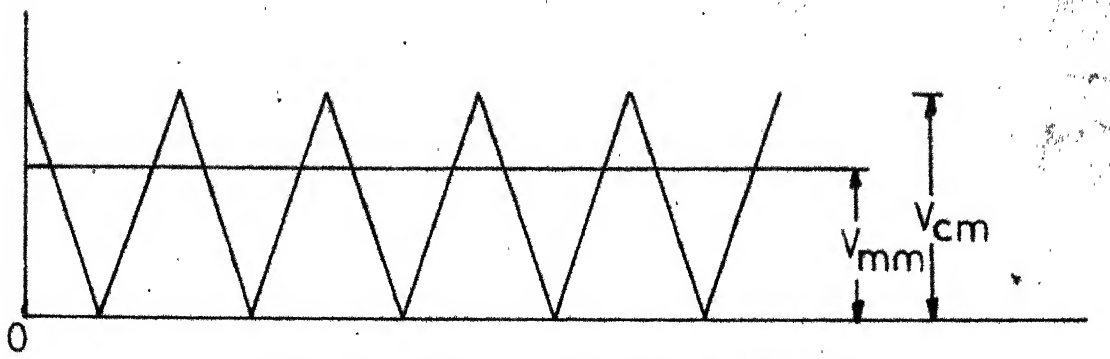
The circuit discussed in Section 2.5 overcomes all the above disadvantages. Even the control circuit requirements are not complex. Hence, this particular circuit is employed for implementing the forced commutation scheme. The converter circuit has been studied with R-L load to a limited extent[5]. A more detailed study of this converter circuit with R-L load is presented simulating the devices by binary logic variables. In spite of the simplicity of the converter circuit, the converter circuit operation with motor load has not been studied. Therefore, an attempt is made to identify different modes of operation of this converter circuit with both R-L and motor load. A separately excited dc motor is used as a load.

CHAPTER III

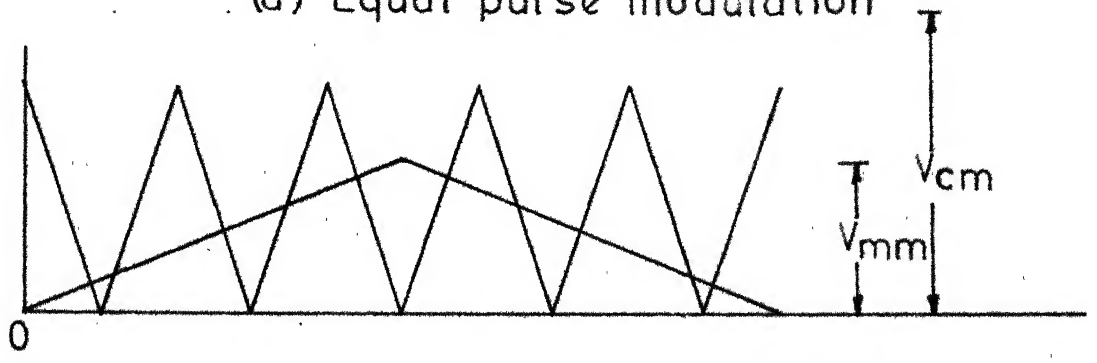
EXTERNAL PERFORMANCE CHARACTERISTICS OF SINGLE PHASE PULSE-WIDTH CONTROLLED CONVERTER

3.1 INTRODUCTION

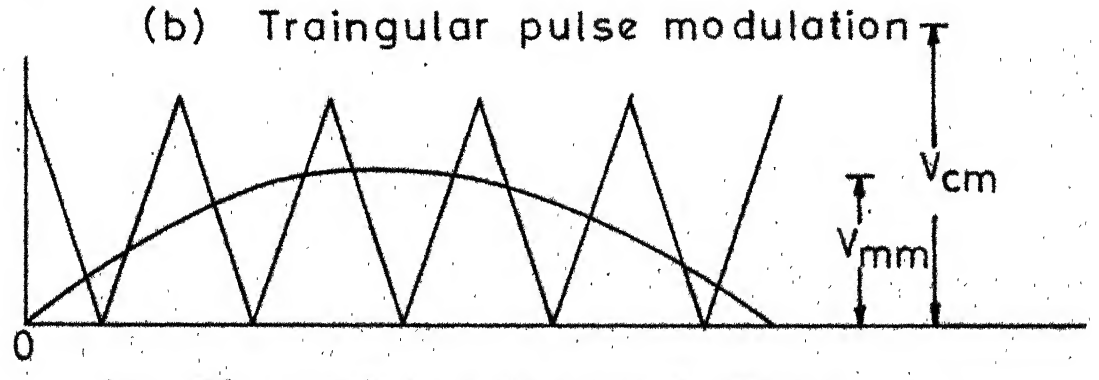
Phase controlled converters have the major disadvantage of poor line power factor at large phase angle delays. Also they generate harmonics in the input ac lines and cause interference besides producing ripple in the output voltage. In recent times forced commutation techniques with pulse-width control have been used to improve upon the line conditions of converter systems. Different pulse-width schemes(as illustrated in Fig. 3.1)can be applied for implementing the forced commutation. The output current and output voltage waveforms depend on the type of modulation scheme adopted. Abrol [6] has made a comparative study of these different modulation schemes based on the performance characteristics, filtering requirements and output copper losses of a single phase ac-dc converter system feeding a RL load. It has been shown [6] that inverted sine modulation (Fig. 3.1(e)) compared to other modulation schemes offers minimum ripple in the output current (minimum copper loss), minimum fundamental output voltage harmonic and maximum range of continuous conduction. The output voltage range is limited in all modulation schemes except the equal-pulse modulation, where



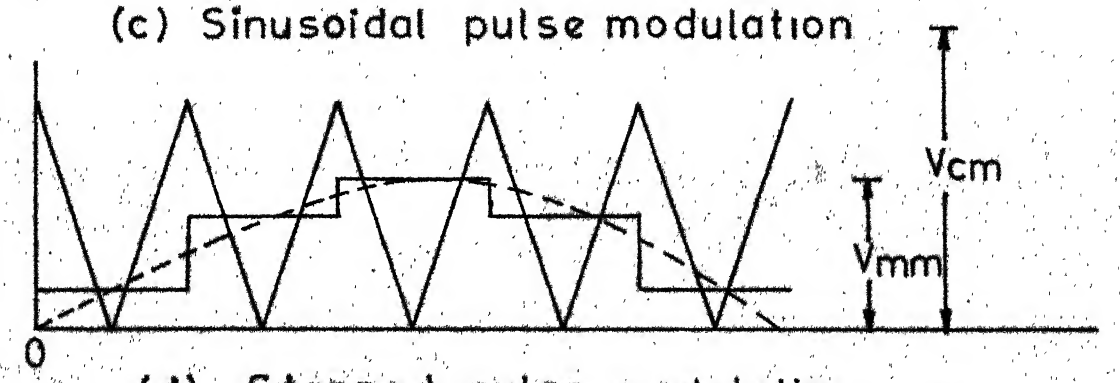
(a) Equal pulse modulation



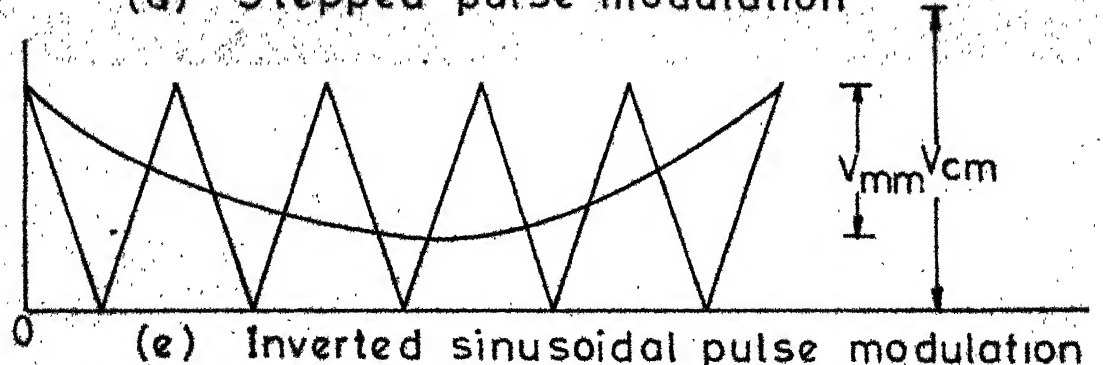
(b) Traingular pulse modulation



(c) Sinusoidal pulse modulation



(d) Stepped pulse modulation



(e) Inverted sinusoidal pulse modulation

FIG. 3.1 DIFFERENT MODULATION SCHEMES

the output voltage variation is from 0 to 100 percent.

Among the inverted-sine and equal-pulse modulation the latter provides maximum output voltage variation and offers better distortion factor than the inverted-sine, without affecting other performances. Therefore 'Equal-pulse' modulation technique, as depicted in Fig. 3.1(a), is employed for the forced commutation of single-phase ac-dc converter.

In this chapter the input line current of single phase ac-dc converter with 'equal-pulse' modulation is analyzed for a motor load. The analysis is carried out using the actual current waveform. Also, the normalized curves are presented showing the continuous and discontinuous armature current conduction regions for different load phase angles on the speed-torque plane. For the sake of comparison, the normalized curves for half controlled converter with conventional phase angle control are also given. Operating diagrams [7] for converter with pulse-width modulation (Equal pulse) are developed. The procedure for calculating the optimum value of filter inductance for continuous current conduction is explained [14, 15].

3.2 DC OUTPUT VOLTAGE RATIO

3.2.1 Output Voltage Waveform

The output voltage waveform of a single phase ac-dc converter for an equal-pulse width modulation is shown in Fig. 3.2., where

$\alpha_1, \alpha_2, \ldots, \alpha_p$ and $\beta_1, \beta_2, \ldots, \beta_n$ are the firing and extinction angles respectively of the main SCRs of converter. These angles are with reference to origin '0'. They depend on the number of pulses 'p' per half cycle.

3.2.2 Determination of Firing and Extinction Angles

The pulses to be given to appropriate SCRs are obtained by the analogue comparison between the carrier voltage of desired frequency and modulating signal as shown in Fig. 3.1. The modulation index 'm' is defined as the ratio of amplitude of modulating signal to the peak amplitude of carrier signal i.e.

$$m = \frac{V_{mm}}{V_{cm}} .$$

The firing angle $\alpha(K)$ and the extinction angle $\beta(k)$ of the kth pulse are defined by the equations :

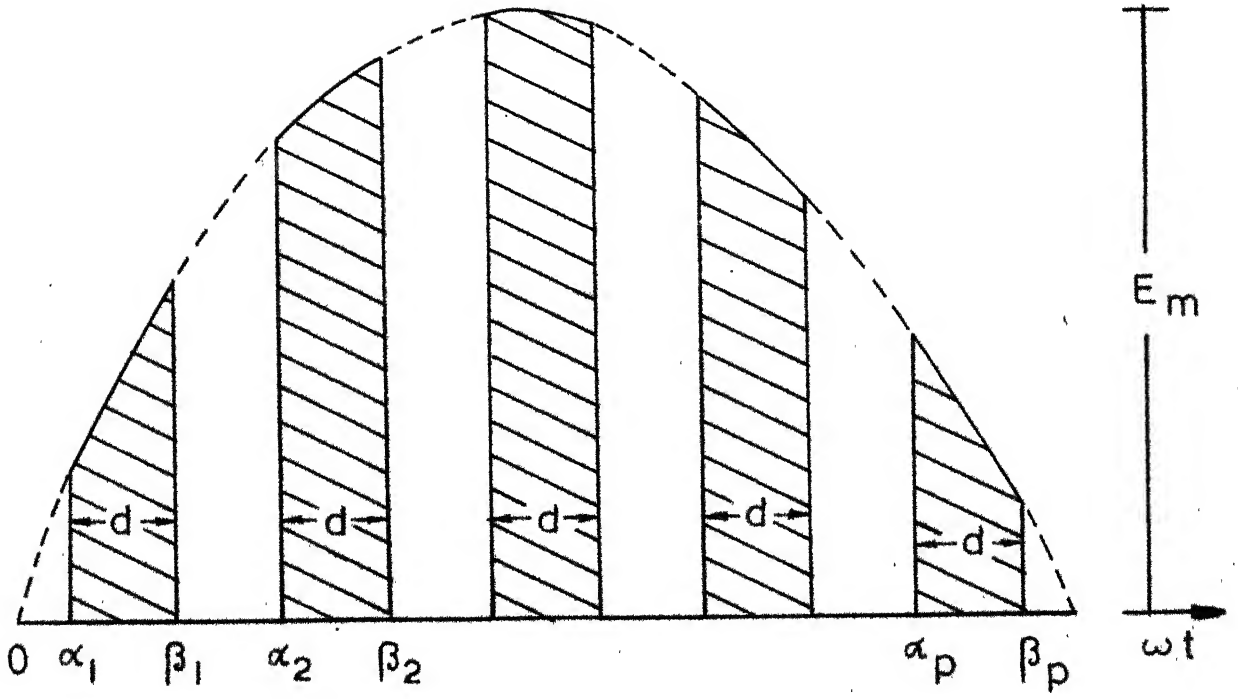
$$V_m(\alpha_k) - V_c(\alpha_k) = 0 \qquad (3.1)$$

and

$$V_m(\beta_k) - V_c(\beta_k) = 0 \qquad (3.2)$$

Eqns. (3.1) and (3.2) give the points of intersection between the modulating signal and the negative and positive slopes of the carrier signal respectively.

For p pulses per half cycle the firing and extinction angles can be found to be [6] ,



Angles $\alpha_1, \alpha_2, \beta_1, \beta_2$ .....are measured from origin 0

α_1 , α_2 ..... α_p firing angles

β_1 , β_2 ..... β_p extinction angles

FIG. 3.2 GENERAL OUTPUT VOLTAGE WAVEFORM OF SINGLE PHASE AC DC CONVERTER WITH EQUAL PULSE WIDTH MODULATION.

$$\alpha(k) = \frac{\pi \cdot (2.k - 1 - m)}{2 \cdot p} \qquad (3.3)$$

and

$$\beta(k) = \frac{\pi \cdot (2 \cdot k + m - 1)}{2 \cdot p} \qquad (3.4)$$

Thus for a particular value of modulation index 'm'and pulse number 'p'the firing and the extinction angles for the different pulses can be found using eqns. (3.3) and (3.4).

3.2.3 Variation of dc Voltage Ratio

From Fig. 3.2 the output voltage function can be defined as

$$v(\theta) = E_m \sin wt \quad \text{for } \alpha_k \leqslant \theta \leqslant \beta_k$$

$$\text{for } k = 1,2, \ldots p$$

$$= 0 \quad \text{for other values of } \theta \qquad (3.5)$$

The dc component of the output voltage is given by

$$v_d = \frac{E_m}{\pi} \cdot \sum_{k=1}^{p} (\cos \alpha_k - \cos \beta_k) \qquad (3.6)$$

The maximum possible output voltage is obtained by substituting $\alpha_k = 0$ and $\beta_k = \pi$ in eqn. (3.6). It is

$$v_{dm} = \frac{2E_m}{\pi} \qquad (3.7)$$

The dc voltage ratio, r is thus given by

$$r = \frac{v_d}{v_{dm}} = \frac{1}{2} \sum_{k=1}^{p} (\cos \alpha_k - \cos \beta_k) \qquad (3.8)$$

Thus it is seen that the dc voltage ratio is a function of firing and extinction angles,which in turn depend upon the number of pulses per half cycle of supply frequency and the modulation index. In order to determine optimum Equal-pulse modulation for linear output voltage variation,the number of pulses are fixed.Firing and extinction angles are calculated using eqns. (3.3) and (3.4),varying m from zero to unity and r is found from eqn. (3.8) for each m. This is repeated for different pulse numbers.

Fig. 3.3 shows the variation in dc voltage ratio with varying modulation index 'm'for different pulse number. Ratio'r' varies almost linearly with modulation index for pulses greater than two. This is quite advantageous when the ac-dc converter is used in a closed loop control system.

3.3 HARMONIC ANALYSIS OF INPUT CURRENT

The harmonic analysis of the input line current is carried out neglecting the commutation transients for the case of continuous conduction. The ac-dc converter is considered ideal, giving the output voltage waveform of Fig. 3.2, which is clearly defined. There are only two modes of operation for the converter circuit. In the power mode, voltage is impressed across the load circuit. In the second mode, when the line voltage is disconnected from the converter circuit, a freewheeling period is initiated by the conduction of appropriate devices of the converter circuit.

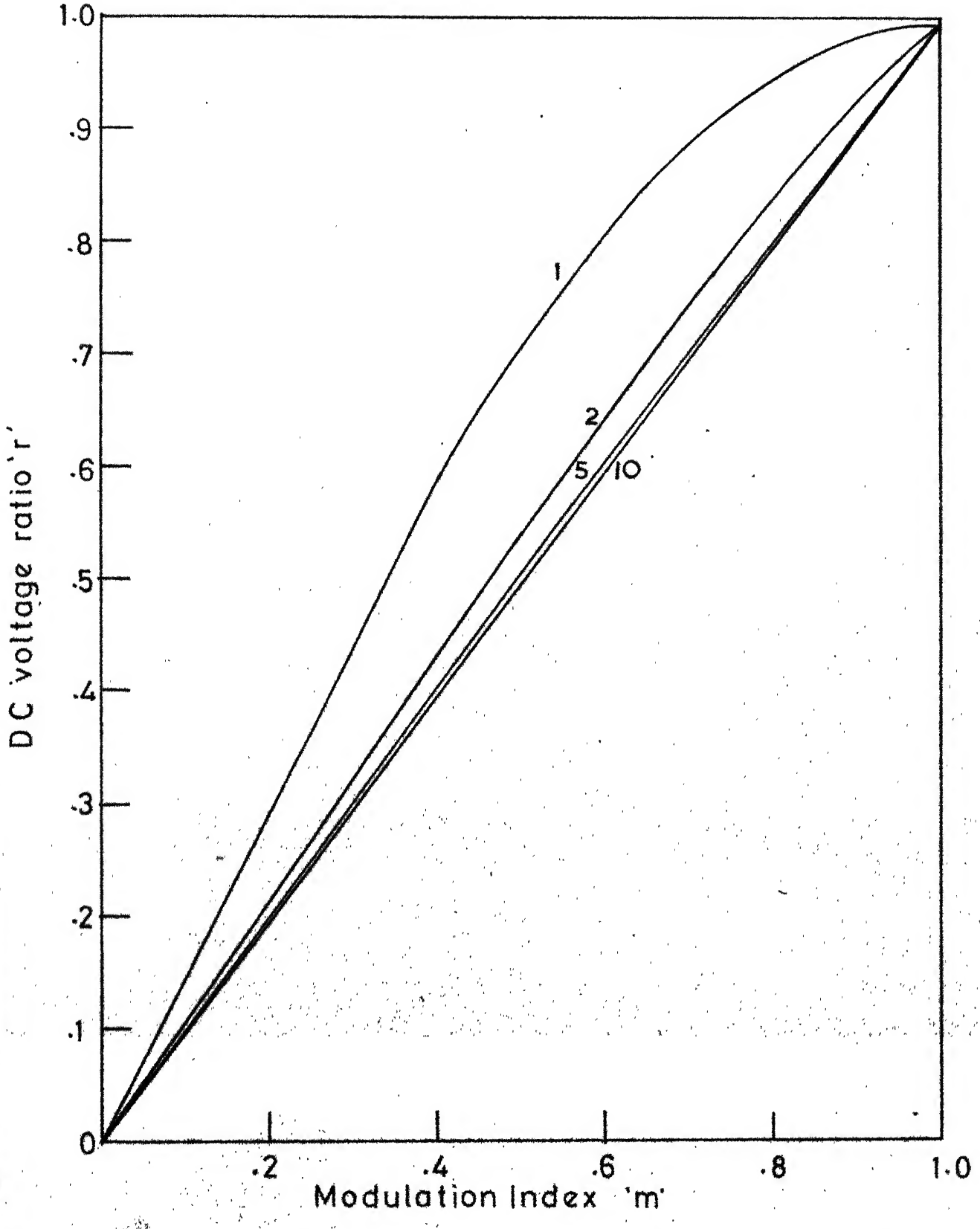


FIG. 3.3 VARIATIONS IN DC VOLTAGE RATIO OF SINGLE PHASE AC-DC CHOPPER

These modes will repeat a number of times during each half cycle depending on the number of pulses. For the above circuit behaviour,the voltage equation for the converter feeding a motor load is,

$$b\ E_m \sin wt = L_t \frac{di_d}{dt} + R_t\ i_d + E \qquad (3.7)$$

where

$E = K_b\ w$ for a seperately excited motor

K_b = Back emf constant

w = speed in rad/sec.

E_m = peak value of ac input voltage

i_d = instantaneous armature current

w = angular frequency of ac supply

L_t and R_t are the total armature circuit inductance and resistance.

b is a constant which is a function of modulation index and number of pulses

$$b = 1 \quad \text{for} \quad |V_m(t)| > |V_c(t)| \qquad (3.8)$$

$$b = 0 \quad \text{for} \quad |V_m(t)| < |V_c(t)| \qquad (3.9)$$

where $V_m(t)$ and $V_c(t)$ are the modulating signal and carrier signal instantaneous magnitudes. From eqn. (3.7),we have

$$\frac{di_d}{dt} = \frac{b\ E_m \sin wt - E - R_t \cdot i_d}{L_t} \qquad (3.10)$$

A numerical method is chosen to solve eqn. (3.10) for finding the steady state instantaneous currents. The analytical solution of eqn. (3.10) becomes quite involved for discontinuous conduction. Even for continuous conduction the analytical solution will require more time for analysis as compared to numerical method. The same method is also utilized for finding the boundary between continuous and discontinuous conduction.

The motor back emf is assumed to be constant over half cycle. The constant 'b' is found using the following equations for the carrier and modulating signals [6] (Fig. 3.1(a)) :

For negative slope of carrier signal and kth pulse

$$v_{c_1}(\theta) = -\frac{1}{\pi}\left[2\,p\theta - \pi\,(2k-1)\right]$$

$$\text{for } \frac{(k-1)\cdot\pi}{p} \leq \theta \leq \frac{(2k-1)\cdot\pi}{2\cdot p}$$

$$\text{and } 0 \leq k \leq p \qquad (3.11)$$

For positive slope of carrier and kth pulse

$$v_{c_2}(\theta) = \frac{1}{\pi}\left[2.p\theta - \pi\,(2k-1)\right]$$

$$\text{for } \frac{(2k-1)\cdot\pi}{2p} \leq \theta \leq \frac{k\pi}{p}$$

$$\text{and } 0 \leq k \leq p \qquad (3.12)$$

For modulating signal

$$v_m(\theta) = m \qquad (3.13)$$

The eqns.(3.11),(3.12) and (3.13) in conjunction with conditions (3.8) & (3.9) give the value of 'b'. The number of pulses and the modulation index are fixed to start with. Some value of load current is assumed, greater than zero (to reduce computer time). The output voltage for a given modulation index and pulse number is calculated from eqn. (3.6). With initial value of load current the differential eqn. (3.10) is integrated with a step size of 50 μsec. The armature current is determined for one half-cycle and its average is calculated. The instantaneous current at the end of half cycle is compared with the value at the beginning of the half cycle. If they are not same, the initial value is updated, and integration carried out. This process is repeated till the convergence is obtained. The convergence of average load current at the end of the half cycle to the value assumed initially is also tested.

After the steady state has resulted, the supply current waveform is analysed by fourier series to determine different harmonics. Also the rms value of supply current is computed. Simpson's rule of integration is used to find the Fourier coefficients, a_n and b_n.

The input performance parameters such as distortion factor 'μ', displacement factor cos φ, power factor and harmonic currents are defined below.

$$\text{Distortion factor } \mu = \frac{\text{rms value of fundamental component}}{\text{rms value of line current component}} \tag{3.14}$$

$$= \frac{(a_1^2+b_1^2)^{\frac{1}{2}}/\sqrt{2}}{I_{rms}} \tag{3.15}$$

where I_{rms} is the supply rms current.

$$\text{Displacement factor } \cos\varphi = \tan^{-1}(-a_1/b_1) \tag{3.16}$$

$$\text{Power factor} = \cos\varphi \times \mu \tag{3.17}$$

$$\text{p.u. harmonic} = \frac{(a_n^2 + b_n^2)^{\frac{1}{2}}}{(a_1^2 + b_1^2)^{\frac{1}{2}}} \tag{3.18}$$

The flow chart for determining the input performances of an ac-dc converter with equal pulse-width modulation is shown in Fig. 3.4(a).

The variations of μ, cos φ, and p.f. with dc voltage ratio 'r' are plotted in Fig. 3.4(b) for two values of load current (full load, half full load). It can be seen from the plots of displacement factor cos φ that it is close to unity for high loads over the entire range of voltage ratio. But it decreases slightly more at reduced loads, with an increase in dc voltage ratio. The power factor increases with an increase in dc voltage ratio. At high voltage ratios, the power factor is

more with higher loads than with lower values of the load. For low dc voltage ratios, the pf is the same for both low and high values of load current. There is no appreciable difference in the distortion factor between low and high values of load current. It increases with an increase in dc voltage ratio.

Fig. 3.4(c) shows the power factor variation with p.u. load current or load torque. It can be seen that for low values of modulation index the maximum available torque decreases. It can be seen that for a particular modulation index the power factor decreases with a decrease in current. Also for a given modulation index, the pf is constant as the current increases.

Fig. 3.5 shows the variation of supply harmonics (upto eleventh) with dc voltage ratio 'r'. From the plots it can be seen that the frequency spectrum shifts from the lower harmonics to the higher harmonics. For the case of pulses greater than seven, all harmonics upto eleventh are considerably reduced (Fig. 3.5(e)).

3.4 CRITICAL INDUCTANCE

3.4.1 Necessity of Additional Load Inductance

For converter fed DC drives, attempts have not only been made to improve line conditions, but also to get a better steady state and dynamic response of the drive. The armature

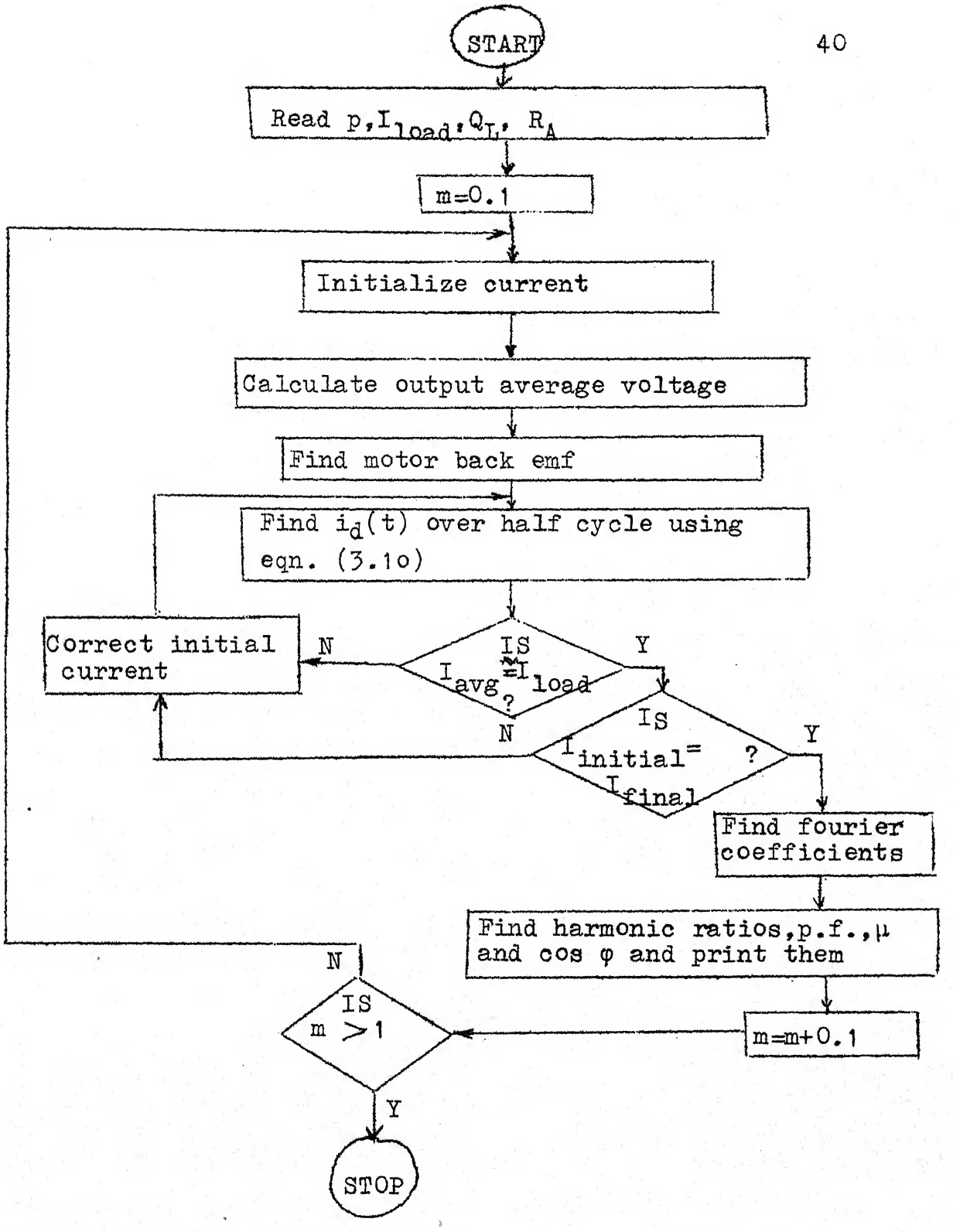


Fig. 3.4(a) Flow Chart for Determining Input Performances of Pulse-width Modulated ac-dc Converter

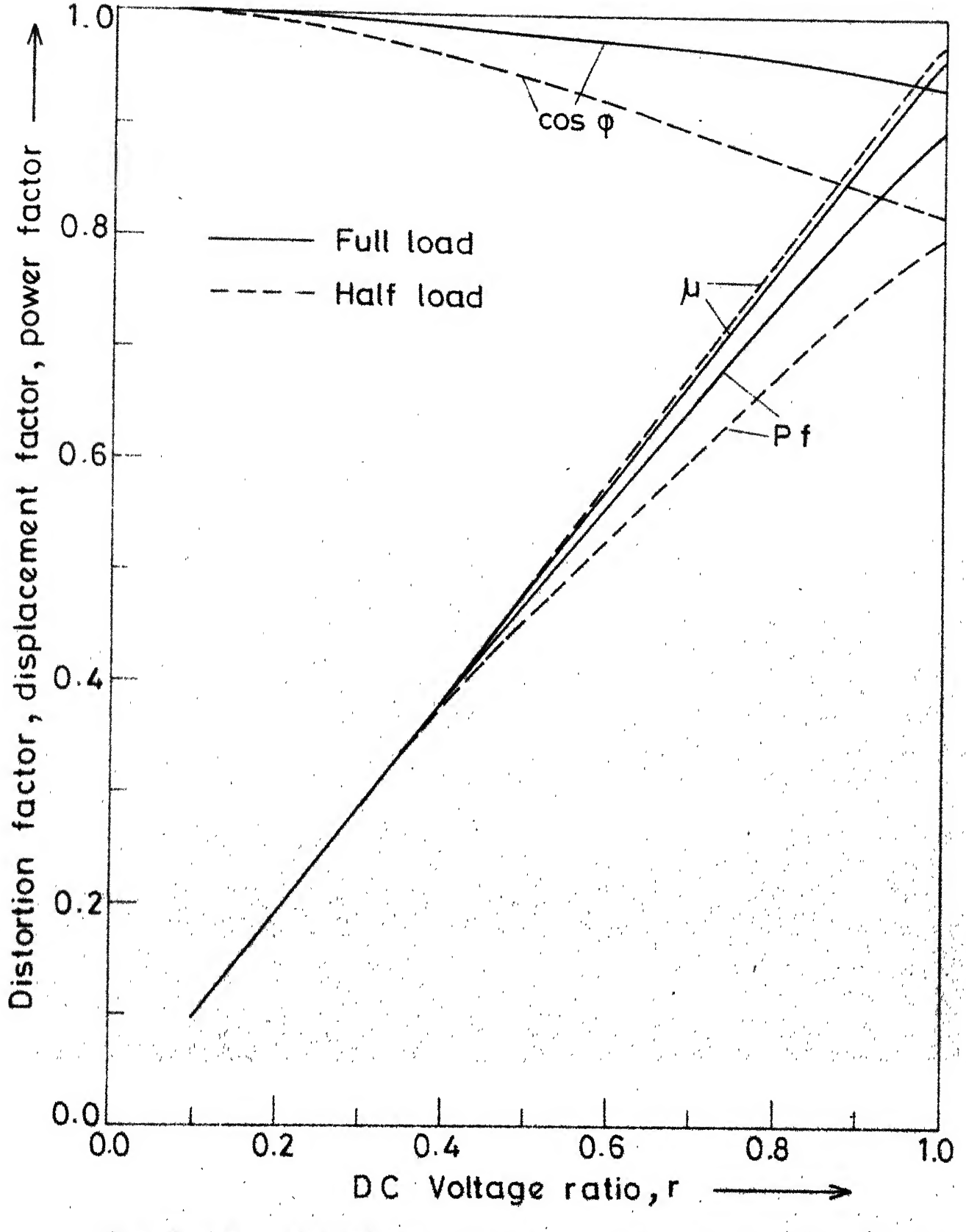
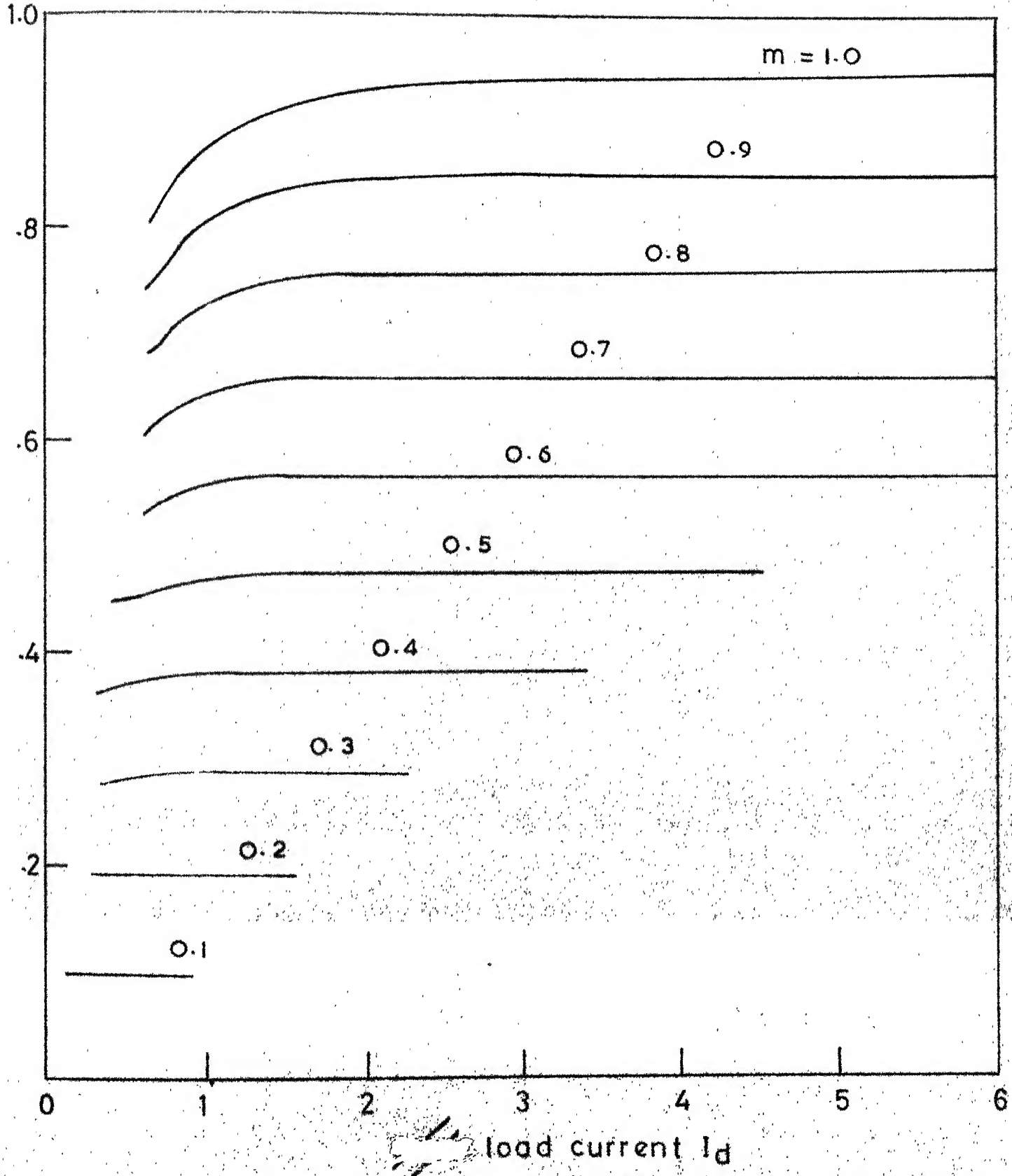
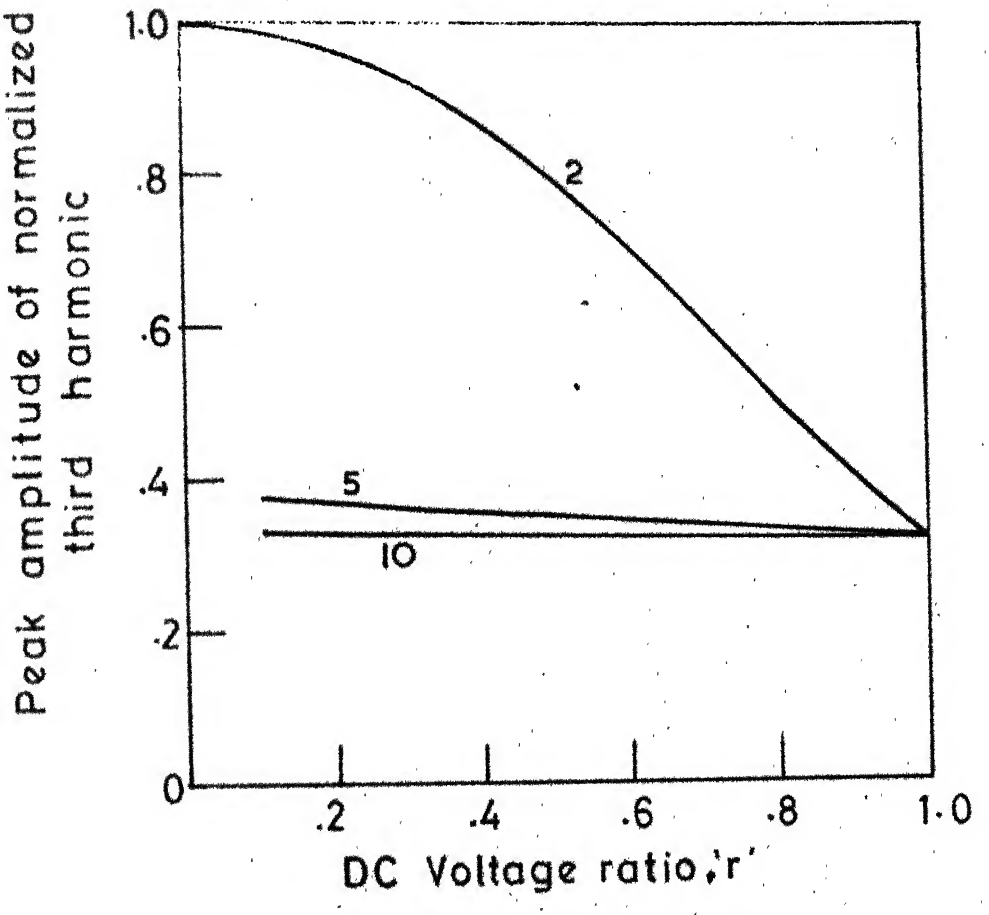


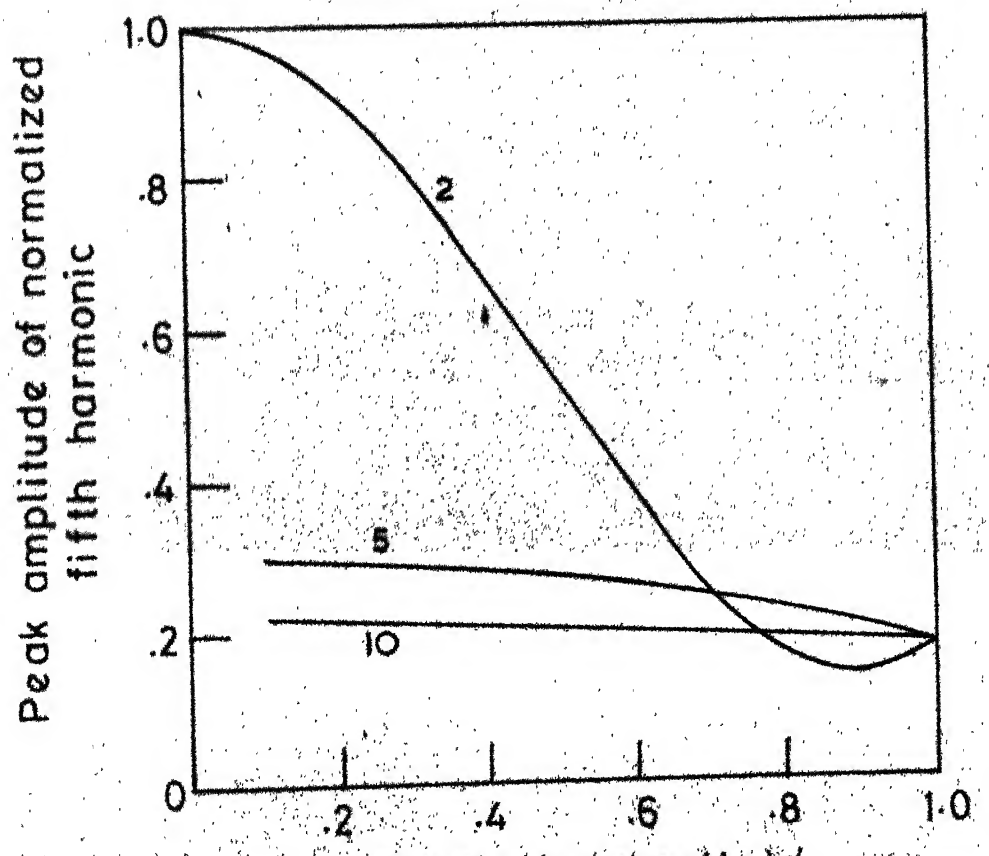
Fig. 3.4b Variations in power factor, distortion factor, displacement factor with 'r' $Q_L = 5.0$



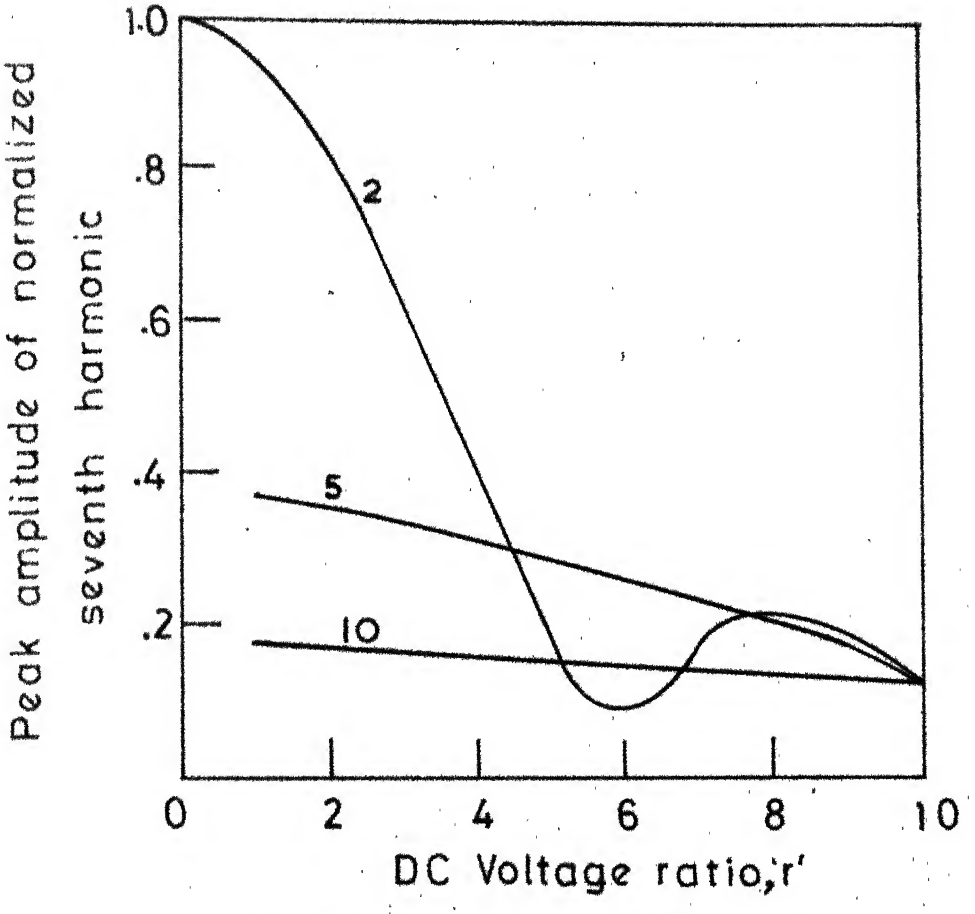
G. 3.4(c) VARIATIONS IN POWER FACTOR WITH LOAD CURRENT $Q_L = 5$



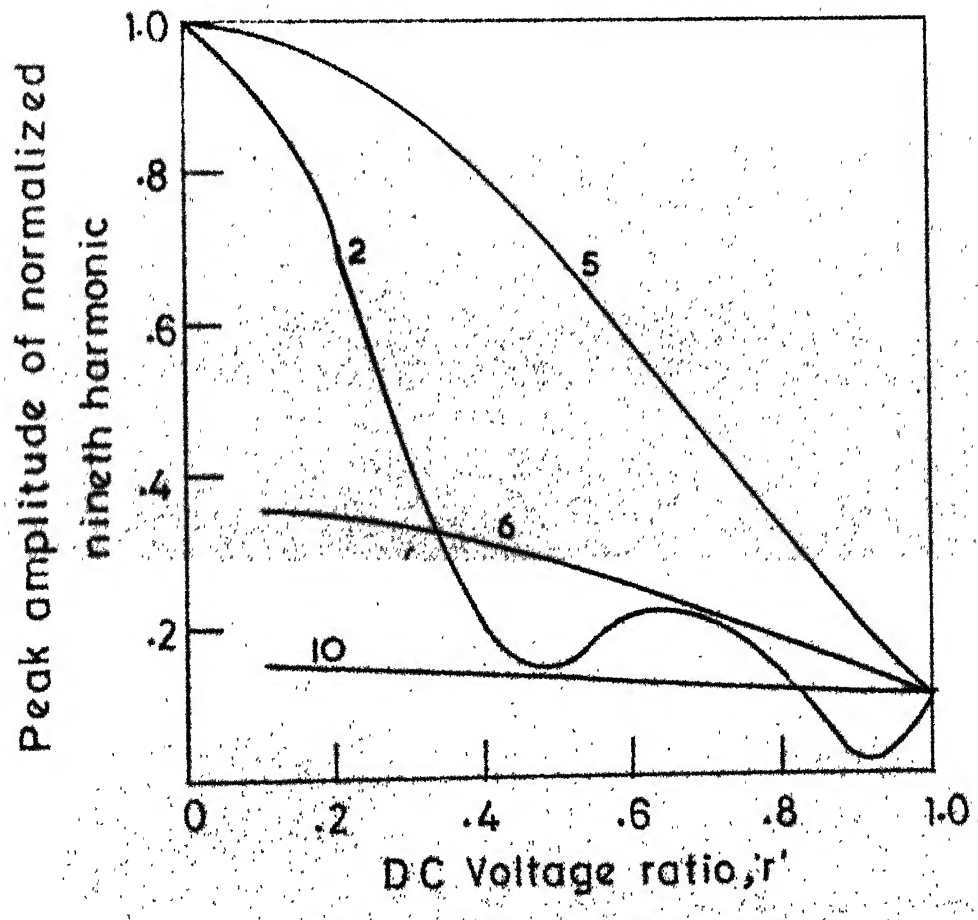
(a) THIRD HARMONIC



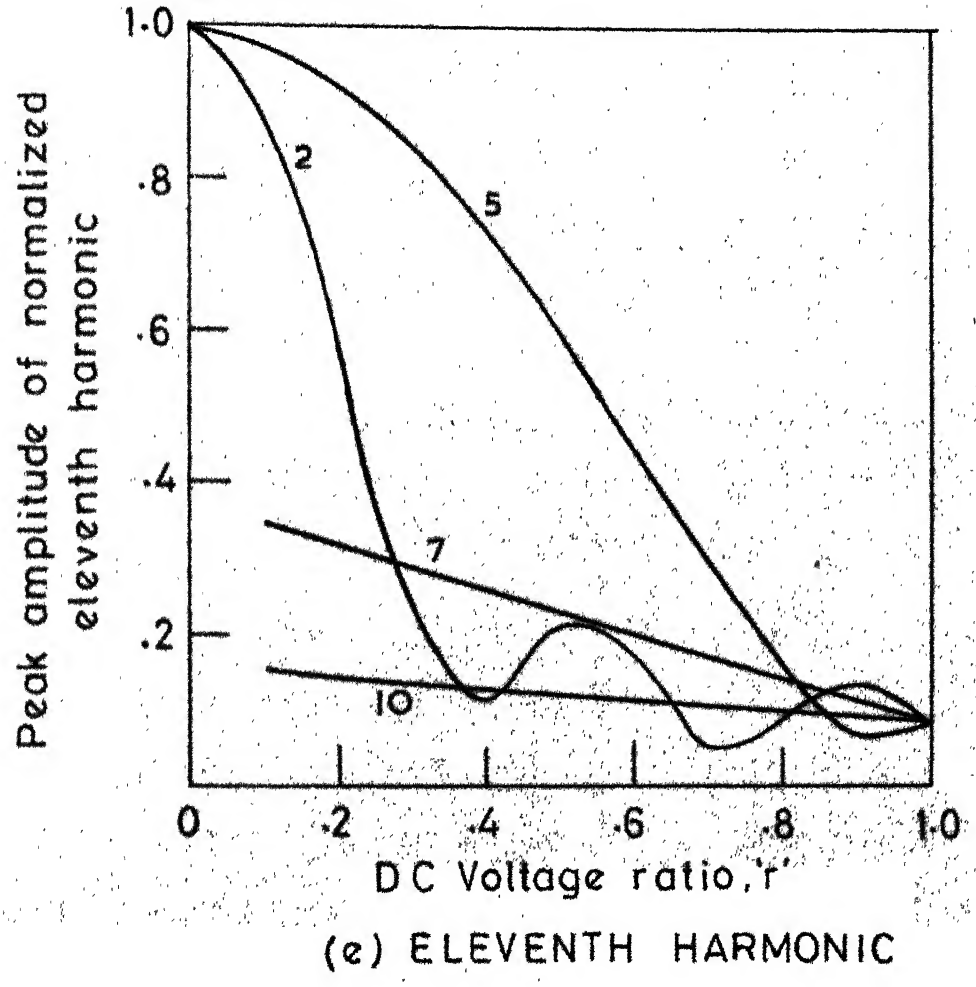
(b) FIFTH HARMONIC



(c) SEVENTH HARMONIC



(d) NINETH HARMONIC



(e) ELEVENTH HARMONIC

FIG. 3·5 VARIATION OF THE LOWER ORDER HARMONICS IN THE INPUT LINE CURRENT WITH DC VOLTAGE RATIO 'r' AT LOAD CURRENT = 11.6 amps. AND QUALITY FACTOR = 5

current may be continuous or discontinuous depending upon modulation index, pulse number and quality factor. This current has a superimposed harmonic ripple. This ac ripple increases losses in motor leading to its derating and reduction in efficiency. At light loads the armature current becomes discontinuous under which speed-regulation becomes poor. An increase in armature circuit inductance results in reduction in ripple and elimination of discontinuous current. An optimum value of the extra inductance required has to be designed as this external inductance reduces efficiency, increases the cost, weight, size and noise. Further it deteriorates the transient response of motor.

3.4.2 Boundary Between Continuous and Discontinuous Conduction

For particular values of load phase angle, φ, modulation index and pulse numbers, the normalized critical speed WN_c and normalised critical torque TN_c are found out. The speed at which the armature current changes from continuous conduction to just discontinuous conduction is defined as critical speed. The torque developed by this current is called critical torque. The armature current is continuous below the critical speed and discontinuous above the critical speed.

The flow chart of Fig. 3.6 explains the procedure for determining the boundary between discontinuous and continuous conduction regions for different pulse nos. Load phase angle,

pulse number and modulation index are initially fixed. Maximum motor speed is assumed initially. The steady state current waveform is determined by solving eqn. (3.10). The current is checked for continuous or discontinuous conduction. If it is discontinuous, the speed is reduced till the current is continuous, whence the critical speed and torque have been reached. The modulation index is changed and the above process is repeated.

The critical torque-speed characteristics for different pulse numbers are shown in Fig. 3.7 for a particular value of load quality factor (=5.8). The current is mostly continuous. The continuous conduction region in the critical speed-torque plane increases with a pulse number greater than 1. There is no appreciable difference as the pulse number is changed from 2 to 10.

Having selected five pulses per half cycle, a set of curves are drawn in Fig. 3.8 (the boundary between continuous and discontinuous conduction for different phase angles shown by solid curves). Also shown in the Fig. 3.8 are a set of curves for a single-phase half-controlled converter [16], for the same load phase angles. These curves show that there is a significant improvement in case of pulse-width controlled ac-dc converter compared to phase controlled converter. For the same load phase angle, the pulse-width

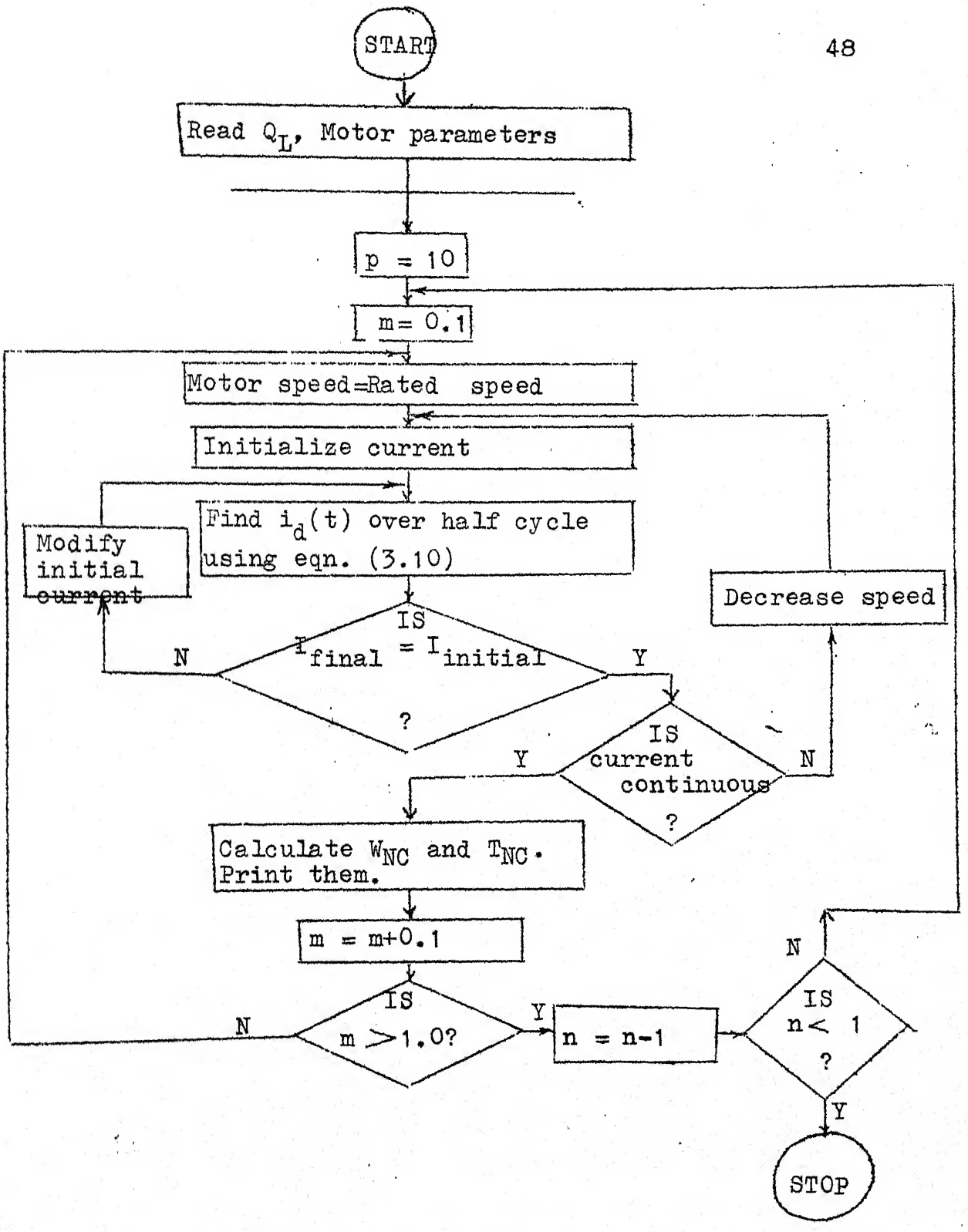


Fig. 3.6 Flow Chart for Finding Boundary Between Continuous and Discontinuous Conduction

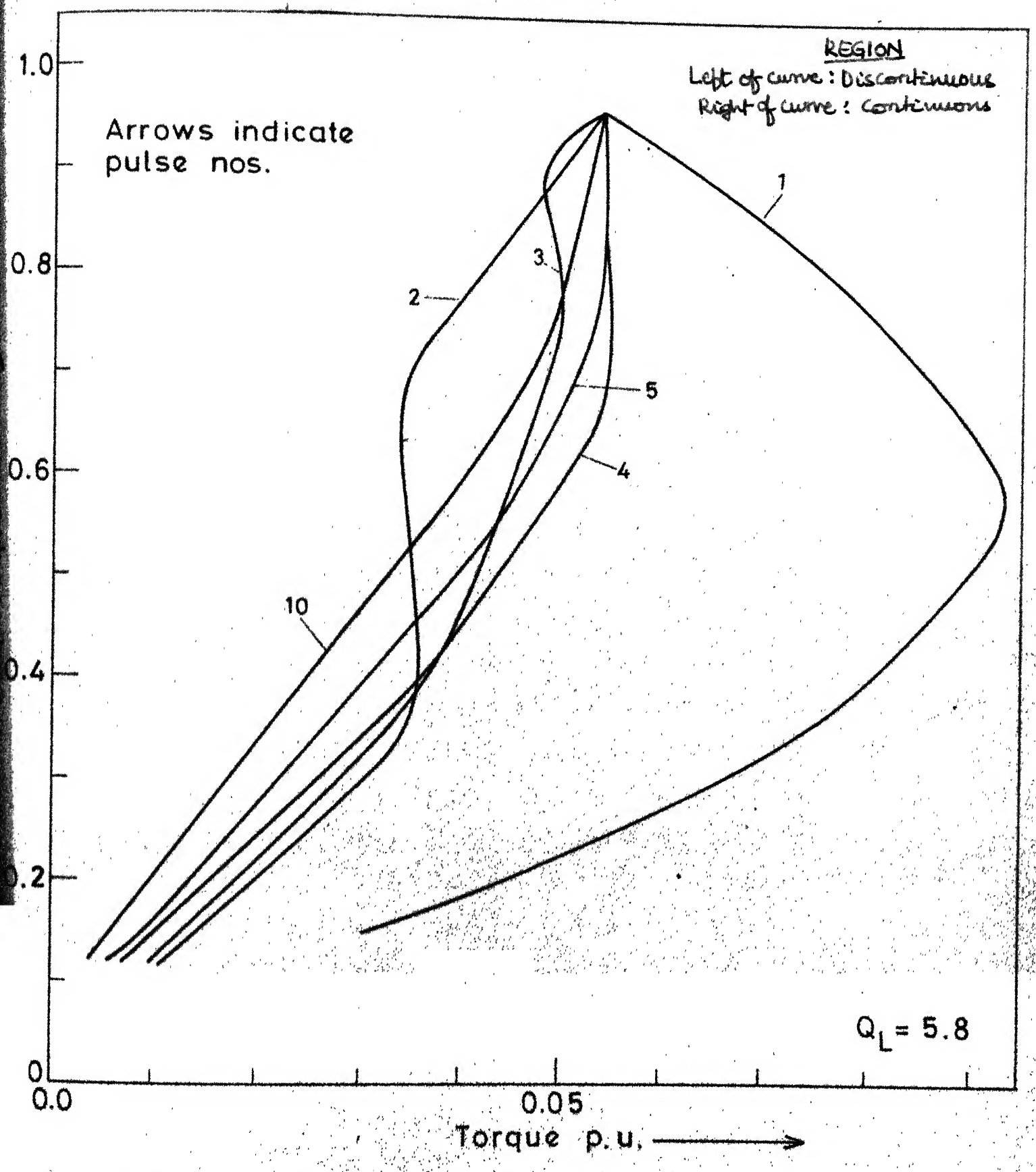


Fig. 3.7 Variation in the boundaries between continuous & discontinuous conduction with pulse nos.

modulated ac-dc converter provides a greater area of continuous conduction region in the speed-torque plane compared to a line commutated half controlled converter. Alternatively,it is possible to operate the pulse-width modulated converter in the continuous conduction mode with a minimum of inductance or with the motor armature inductance itself.

3.4.3 Choice of Filter Inductance

Discontinuous conduction generally occurs at light loads. If continuous conduction is assured for the minimum load at which the drive system is likely to operate over the entire speed range of operation, the load current will be continuous at all loads and speeds. Thus from the load requirements for a particular application under consideration, the minimum values of developed torque are obtained for various speeds and this speed-torque behaviour is superimposed on the curves of Fig. 3.8. Let us consider a typical load characteristic as shown by the chain line. The filter inductance is chosen such that the boundary between continuous and discontinuous conduction lies to the left of this curve [14].

For the load curve shown in Fig. 3.8,the boundary with $\varphi = 0.5$ is suitable if the motor is fed by an ac-dc converter with pulse-width modulation,whereas for the same motor and load fed by a half controlled line commutated converter, the boundary with $\varphi = 0.8$ is suitable. This clearly shows that

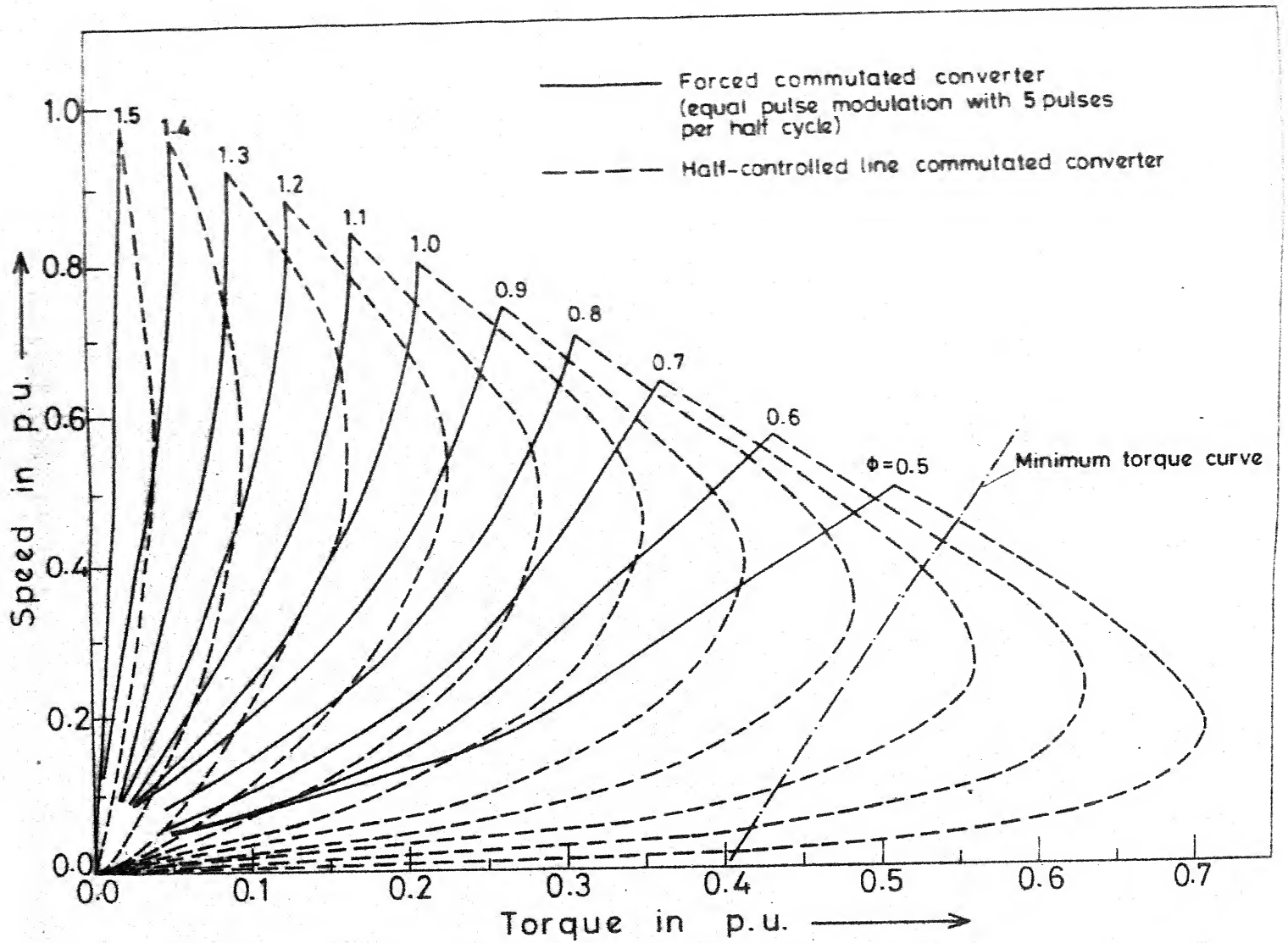


Fig. 3.8 Boundaries between continuous and discontinuous conduction for AC-DC converter

with a smaller filter inductance, the pulse width controlled ac-dc converter provides a continuous conduction compared to a line commutated converter. Consequently, pulse-width controlled ac-dc converter provides higher efficiency, fast time response besides improving the input ac performances compared with a conventional phase-controlled converter. Also with a small filter inductor, the cost, weight, size and noise will be less.

3.4.4 Operating Diagrams and Minimum Inductance Calculation

The operating diagrams for the rectification mode can be obtained as explained in the flow chart of Fig. 3.6 for various values of load angle. These operating diagrams [ ], which show the possible and permissible conditions of operation of a pulse-width modulated ac-dc converter, are shown in Fig. 3.9(a). The load may be a motor or a battery.

These operating diagrams can also be utilized for finding the critical inductance required [15], by means of a graphical method. For the load angle 45° and modulation index 0.8, the ordinate XY is the normalized back emf at the continuous conduction limit and XZ gives the normalized output voltage of ac-dc converter. Thus YZ gives the normalized resistive drop at the limit of continuous conduction. The normalized drop ($I_d R_a/E_m$) is plotted against the modulation index 'm'

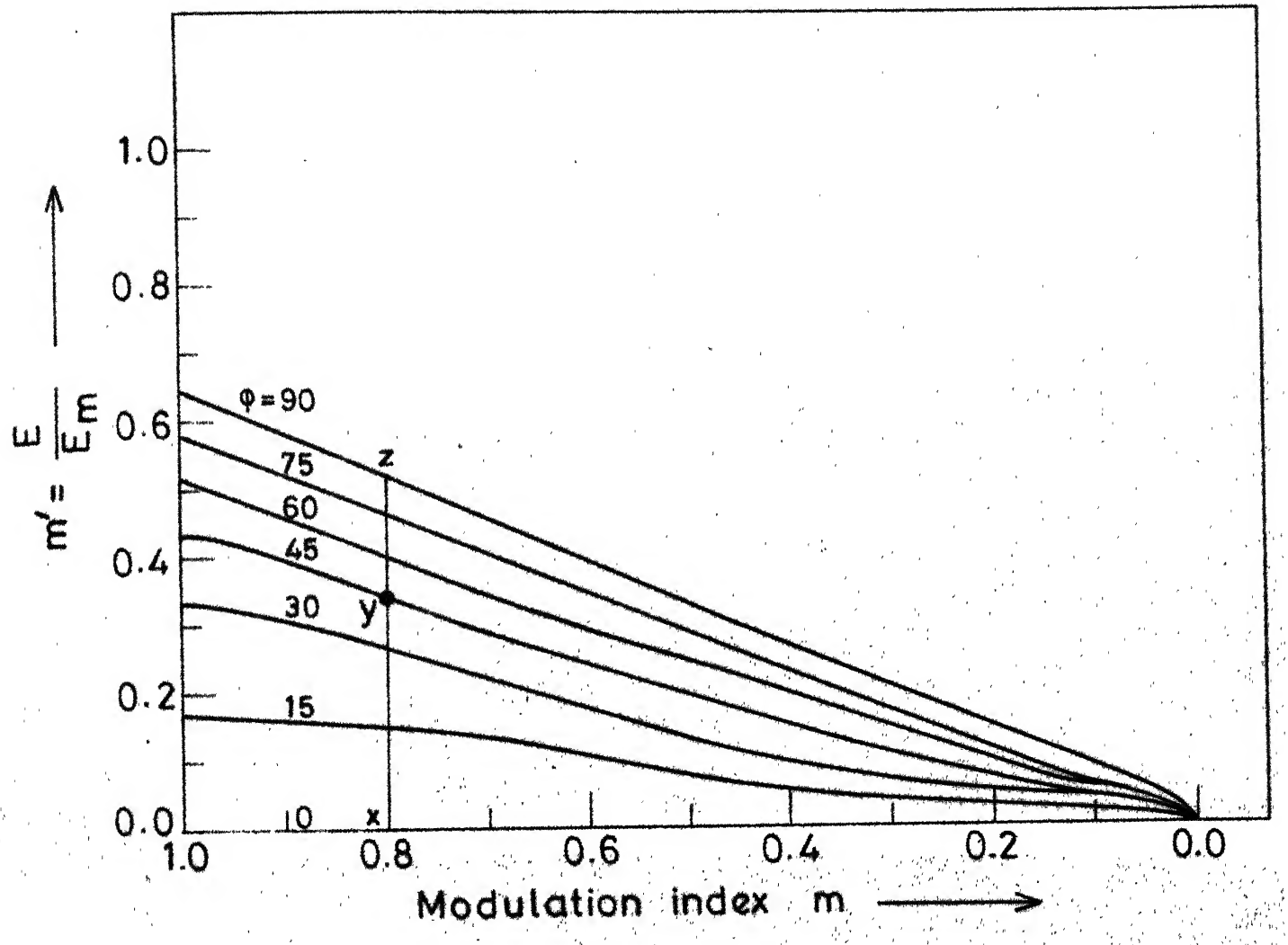


Fig. 3.9(a) Operating diagram for rectification.

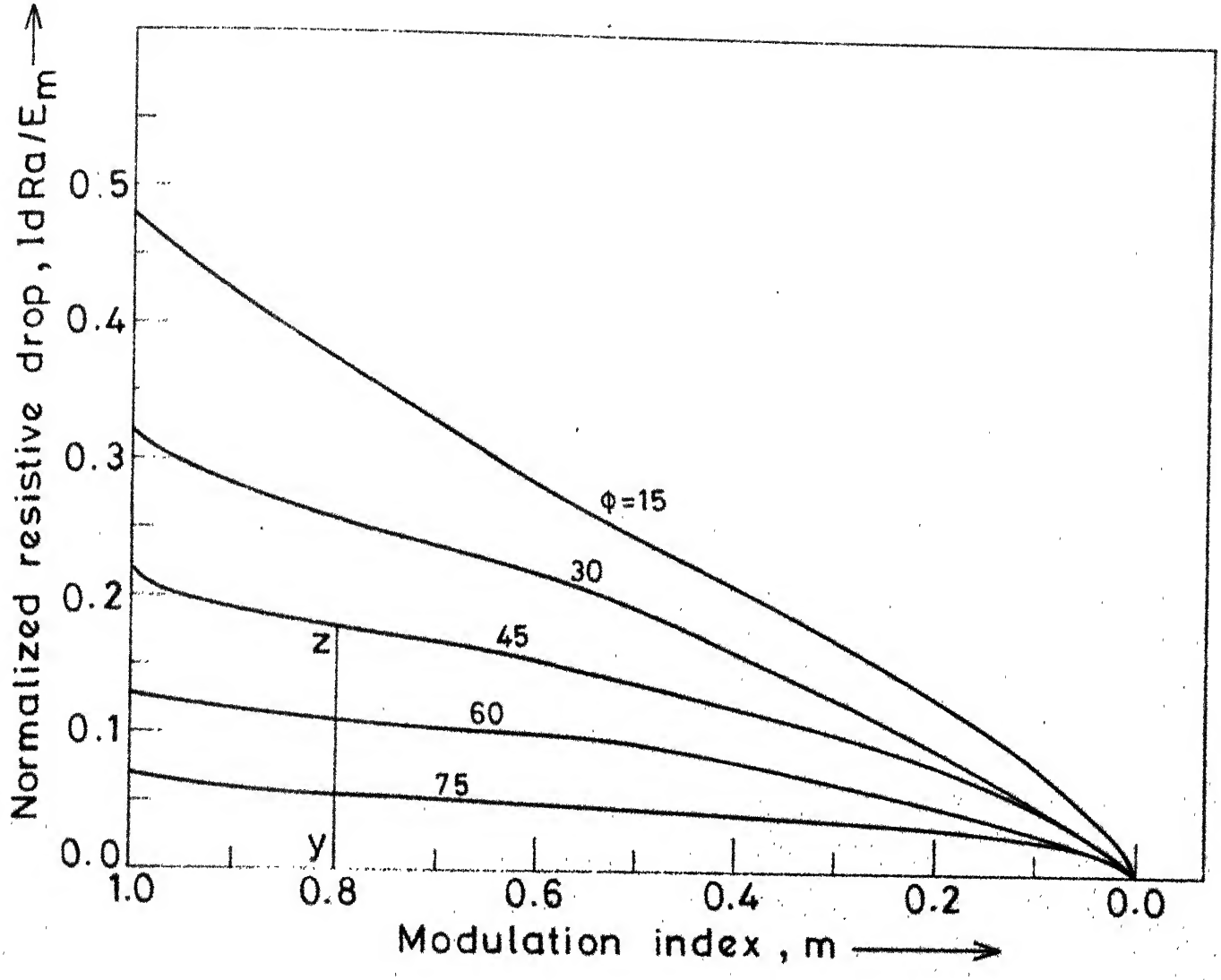


Fig. 3.9(b) Variation in normalised resistive drop with m and for various values of load angle.

for different values of 'φ'as shown in Fig. 3.9(b). Knowing the output current, 'm', and armature resistance, the minimum value of load phase angle 'φ'for continuous conduction can be chosen. Knowing the load circuit inductance, the additional inductance required can be calculated. These diagrams can be used for estimating minimum inductance for continuous conduction with R-L load and battery type of loads. The procedure explained in Section 3.4 can be readily applied for motor loads.

3.5 CONCLUSIONS

It is seen that the output voltage variation with the modulation index is quite linear for pulse number greater than 2. This is quite advantageous when the ac-dc converter is used in a closed loop scheme. For pulse number less than seven and greater than three the frequency spectrum shifts from the lower order harmonics to the higher order harmonics in the input line current. These higher order harmonics can be easily filtered out. For pulse number greater than five the lower order harmonics (upto the 11th) are reduced considerably but for pulses more than five the range of output voltage variation is limited because of the time constraint of the turn off time of SCR. Five pulses in each half cycle seems to be an optimum number from the considerations of output voltage linearity, and minimization of lower order harmonics and large output voltage variation range. The

armature current in a PWM converter is mostly continuous but becomes discontinuous for very light loads. In order to make the current continuous even at light loads it is seen that the inductance required in much less in a PWM AC-DC converter as compared to a phase controlled converter. This increases the efficiency and improves transient response besides minimising cost, size, weight and noise.

CHAPTER IV

ANALYSIS OF AC-DC CONVERTER WITH FORCED COMMUTATION

4.1 INTRODUCTION

It is most convenient to use digital computation to analyse thyristor controlled circuits for several reasons :

1. The steady state as well as the transient performance can be predicted fast on a digital computer.

2. The input data can be easily changed to take account of different element values and/or different initial conditions.

3. The computation logic is quite similar for different thyristor circuits.

The most common method of computer aided analysis of SCR circuits is to formulate differential equations for the different equivalent circuits arising due to different active devices conducting (which are considered as ideal switches). The state variable approach is used,which gives minimum number of equations. These equations alongwith the initial conditions(at mode changeover points)and the variables are computed digitally.

The above method suffers from a severe drawback, in that, the modes should be known apriori, but generally the exact

circuit behaviour is not known apriori and hence thyristor circuit analysis can be tackled only by simulation at device level in a digital computer.

In this chapter the various modes of operation of pulse-width controlled ac-dc converter shown in Fig. 4.3 are analysed for both passive and active loads. The passive load consists of a R-L while the active load comprises a separately excited dc motor. The lumped circuit model as explained in Appendix I is adopted for the motor. The effect of commutation phenomenon on the torque-speed characteristic is investigated. As discussed in Chapter 3, the pulse-width control scheme with five pulses per each half cycle of supply voltage appears to be optimum. The converter is analysed with ten pulses (500 Hz) in each supply cycle. The commutation effect on the speed-torque characteristics is also investigated. The converter operates in the continuous current conduction mode (Chapter 3) for most practical operating conditions and therefore the results are presented for the case of continuous conduction.

4.2 SIMULATION OF THYRISTOR AND DIODES

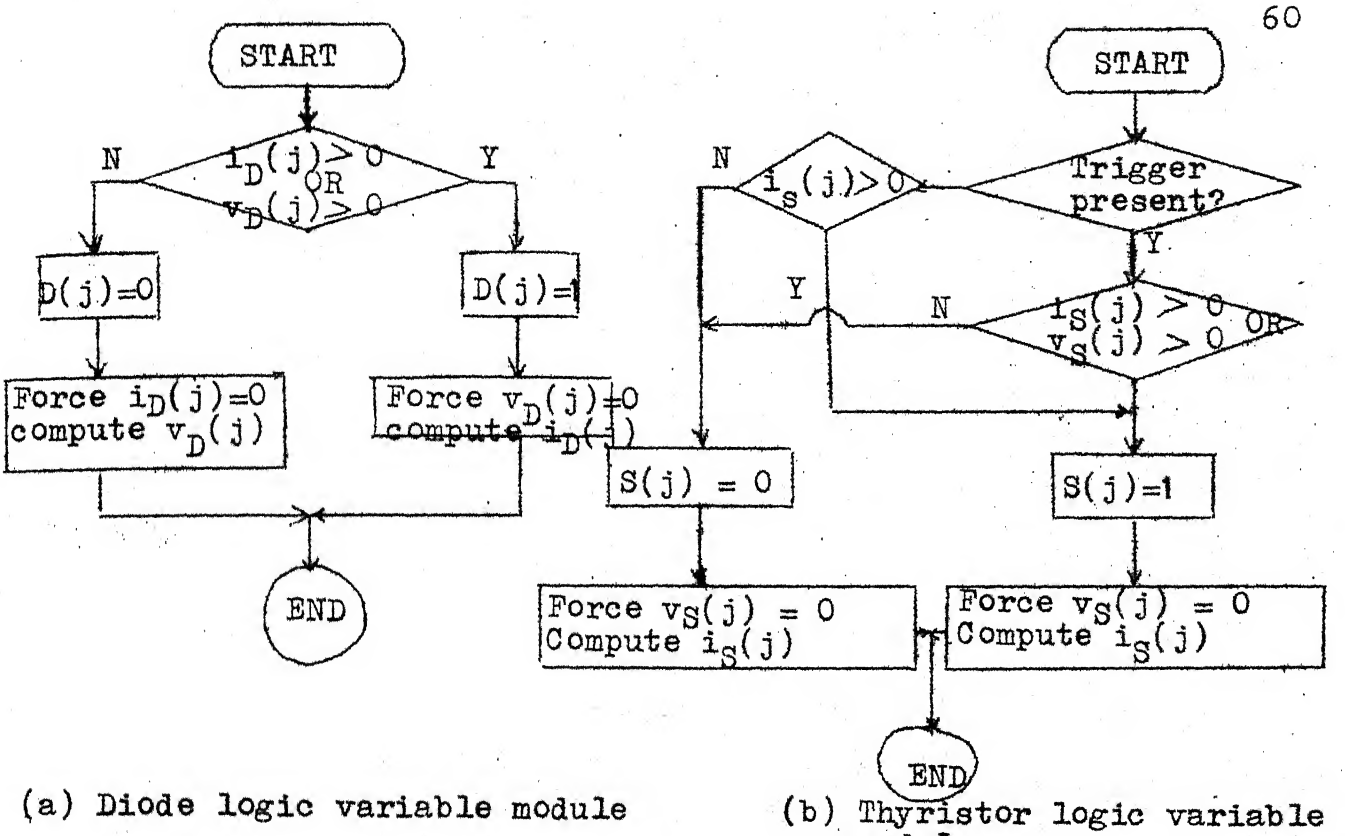
The devices can be simulated by two methods. These are :

(i) The devices are considered as ideal switches i.e. when a device is ON it represents zero resistance and when it is OFF it represents an open circuit condition. In a diode the positive anode to cathode voltage determines the ON state

whereas in an SCR this has to be coupled with the presence of gate pulse. Once the device starts conducting, it continues to do so till its current becomes zero or negative. The logic modules are shown in Fig. 4.1.

S(j) and D(j) are used to describe the binary state of the jth device, which can have a value 0 or 1 depending on whether the device is in ON or OFF state. These variables are used with the device current and voltage and the state variable equations. These equations are modified according to the value of the logic variables. If the device is OFF, the device current is forced to zero and voltage across the device is found while if the device is ON the device voltage is forced to nearly zero and the current through it is found, both the forcings being done by logic variables for the particular device. The state equations are written in terms of state variables, circuit parameters, logic variables and device voltages. These state equations are digitally computed and at the beginning of each iteration the device current and voltage are computed. If there is a change in mode (different devices conducting), the details showing the new incoming mode are indicated.

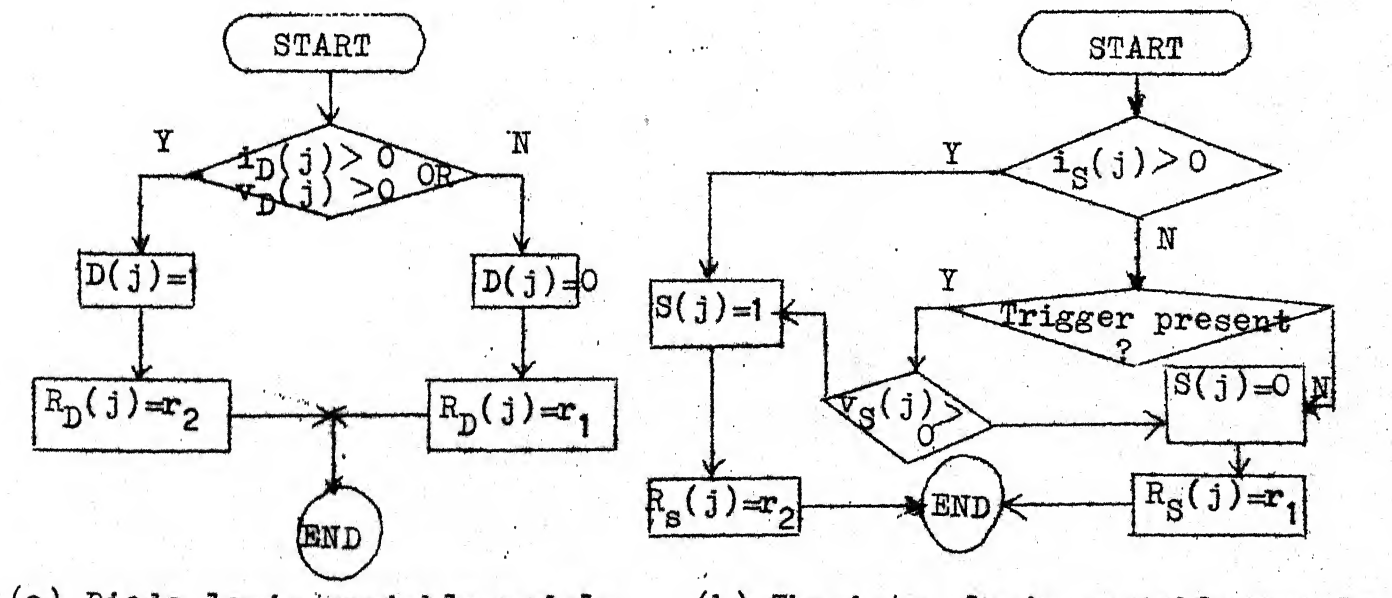
(ii) In this method, when the device is ON the device is represented by a very low resistance and when the device is OFF it is represented by a resistance depending on the ON-OFF condition of the device. The logic modules are shown in Fig. 4.2.



(a) Diode logic variable module

(b) Thyristor logic variable module

Fig. 4.1 Ideal Switch Representation



(a) Diode logic variable module

(b) Thyristor logic variable module

Fig. 4.2 Binary Resistance Representation

The first method of simulation [17] involves less computer time and no instability problem arises while in the second method , the resulting differential equations are stiff and require very large integrating time using conventional methods. The error involved depends on choice of method of integration and the numerical value of the binary resistance. Hence, the first method of device simulation is followed in the analysis of the pulse-width controlled AC-DC converter.

4.3 FORMULATION OF GENERALIZED STATE EQUATIONS

Equations are developed for only one half cycle as the next half cycle is just the repetition of the previous half cycle with only the following changes.

(a) Capacitor voltage polarity will be reversed.

(b) Currents in SCRs S_1 and S_2 (Fig. 4.3) will be interchanged.

(c) The currents in diodes D_1 and D_2 (Fig. 4.3) will also be interchanged.

Referring to Fig. 4.3 the following parameters are chosen as state variables.

$$Z_1 = i_{L_1},\ Z_2 = i_{L_2},\ Z_3 = i_d,\ Z_4 = V_c,\ Z_5 = i_s.$$

Let the drop across a thyristor be V_S and drop across diode be V_D. The currents and voltages shown in Fig. 4.3 are assumed to be positive. It can be inferred from the converter circuit of Fig. 4.3 that,

I. S_1 and S_2 cannot conduct simultaneously as they will give rise to commutation failure and so is the case with S_3 and S_4.

II. D_{L_2} can conduct only when S_1 conducts as it forms a closed loop with S_1 in series.

III. Similarly D_{L_1} can conduct only when S_2 conducts.

4.3.1 Calculation of $\dot{Z}_1$

The only loop possible is shown in Fig. 4.3.1. Applying KVL to loop formed by D_{L_1}, L_1, C and S_2 we get

$$Z_4 - V_{S_2} - V_{D_{L_1}} - L_1 \cdot \dot{Z}_1 = 0 \quad \text{if} \quad S(2) = D_L(1) = 1 \qquad (4.1)$$

Therefore,

$$\dot{Z}_1 = \frac{1}{L_1} \left[Z_4 - V_S - V_D\right] \; S(2) \; D_L(1) \qquad (4.2)$$

4.3.2 Calculation of $\dot{Z}_2$

The only loop possible is shown in Fig. 4.3.2. Applying KVL to loop formed by S_1, C, L_2, and D_{L_2} we get

$$Z_4 + V_{D_{L_2}} + V_{S_1} + L_2 \dot{Z}_2 = 0,$$
$$\text{if } S(1) = D_L(2) = 1 \ldots \qquad (4.3)$$

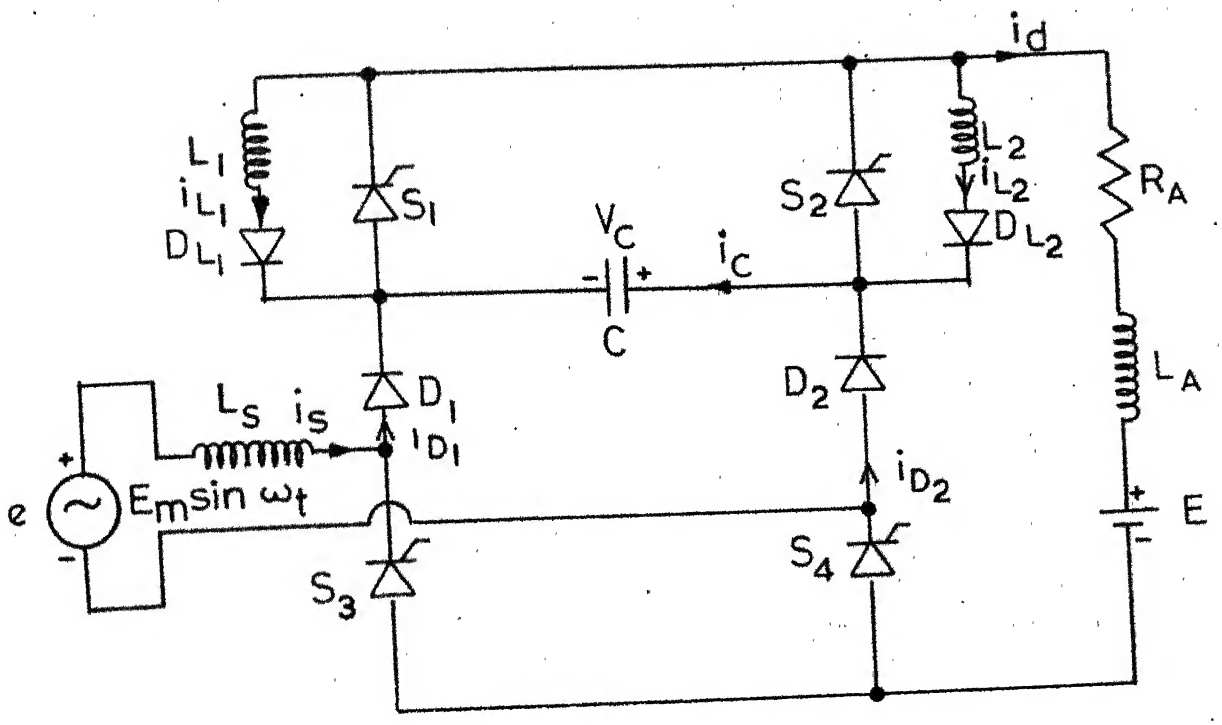


FIG. 4.3 1ϕ AC-DC CONVERTER CIRCUIT

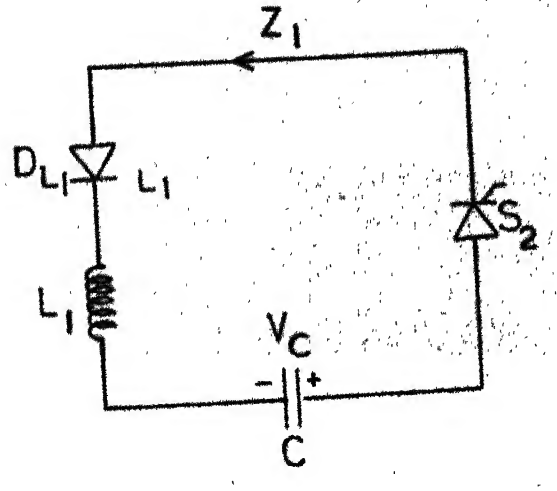


FIG. 4.3.1 LOOP FOR STATE VARIABLE Z_1

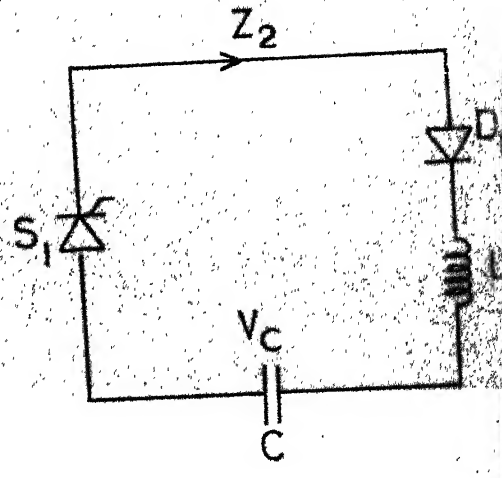


FIG. 4.3.2 LOOP FOR STATE VARIABLE Z_2

Therefore,

$$\dot{Z}_2 = -\frac{1}{L_2}\,[Z_4+V_D+V_S] \cdot S(1) \cdot D_L(2) \ldots \qquad (4.4)$$

4.3.3 Calculation of $\dot{Z}_3$

The various possible loops are shown in Fig. 4.3.3. Let us consider them one by one.

(a) Applying KVL to Fig. 4.3.3(a) we get

$$E_m \sin wt - L_s\dot{Z}_3 - V_{D_1} + Z_4 - V_{S_2} - Z_3 R_A - L_A \dot{Z}_3 - E - V_{S_4} = 0$$

$$\text{if } D(1) = S(2) = S(4) = 1 \ldots \qquad (4.5)$$

$$(L_A+L_s)\dot{Z}_3 = (E_m \sin wt + Z_4 - R_A Z_3 - E - V_D - 2V_s) \cdot$$

$$D(1)\ S(2)\ S(4)\ (D(1)-D(2)) \qquad (4.6)$$

(b) Applying KVL to Fig. 4.3.3(b) we get

$$E + L_A \dot{Z}_3 + R_A Z_3 + V_{S_2} + V_{D_2} + V_{S_4} = 0$$

$$\text{if } D(2)=S(2) = S(4) = 1 \qquad (4.7)$$

$$L_A \dot{Z}_3 = -(E + R_A Z_3 + 2 V_S + V_D) \cdot D(2)\ S(2)\ S(4)\ (D(2)-D(1)) \qquad (4.8)$$

(c) Applying KVL to Fig. 4.3.3(c) we get

$$E + L_A \dot{Z}_3 + R_A Z_3 + V_{S_1} + Z_4 + V_{D_2} + V_{S_4} = 0$$

$$\text{if } D(2) = S(4) = S(1) = 1 \qquad (4.9)$$

$$L_A \dot{Z}_3 = -[E+R_A Z_3 + Z_4 + 2V_S+V_D]\ S(1)\ S(4)\ D(2)\ (D(2)-D(1)) \qquad (4.10)$$

(d) Applying KVL to Fig. 4.3.3(d) we get

$$E_m \sin wt - L_s \dot{Z}_3 - Z_3 R_A - L_A \dot{Z}_3 - E - V_{S_4} - V_{D_1} - V_{S_1} = 0$$

$$\text{if } S(1) = S(4) = D(1) = 1 \qquad (4.11)$$

$$(L_A+L_s)\ \dot{Z}_3 = (E_m \sin wt - Z_3 R_A - E - 2V_S - V_D)\ S(1)\ S(4)\ D(1) \cdot$$

$$\cdot\ (D(1) - D(2)) \qquad (4.12)$$

Combining equations (4.6), (4.8), (4.10) and (4.12) and simplifying we get

$$\dot{Z}_3 = D(1)\ S(4)\ (D(1)-D(2)) \cdot [(E_m \sin wt + Z_4 - R_A Z_3 - E - V_D - 2 V_S)\ S(2)$$

$$+ (E_m \sin wt - Z_3 R_A - E - 2 V_S - V_D)\ S(1)]/(L_A+L_s)$$

$$- (D(2)\ S(4)\ (D(2)-D(1)) \cdot [(E + R_A Z_3 + 2 V_S + V_D)\ S(2)$$

$$+ (E + R_A Z_3 + 2 V_S + Z_4 + V_D)\ S(1)]/L_A \qquad (4.13)$$

4.3.4 Calculation of $\dot{Z}_4$

The various possible loops are shown in Fig. 4.3.4.

(a) Applying KCL to Fig. 4.3.4(a) at Node A, we get

$$i' = -i_c = i_{L_1} + i_d \quad \text{if } D(1) = S(2) = S(4) = 1 \text{ and}$$

$D_{L_1}(1) = 1$ also D(2) may be one alongwith D(1)=1, but not alone. (4.14)

$$i_c = C\dot{Z}_4 = -(Z_3\ D(1)\ S(2)\ S(4) + Z_1\ D_L(1)) \qquad (4.15)$$

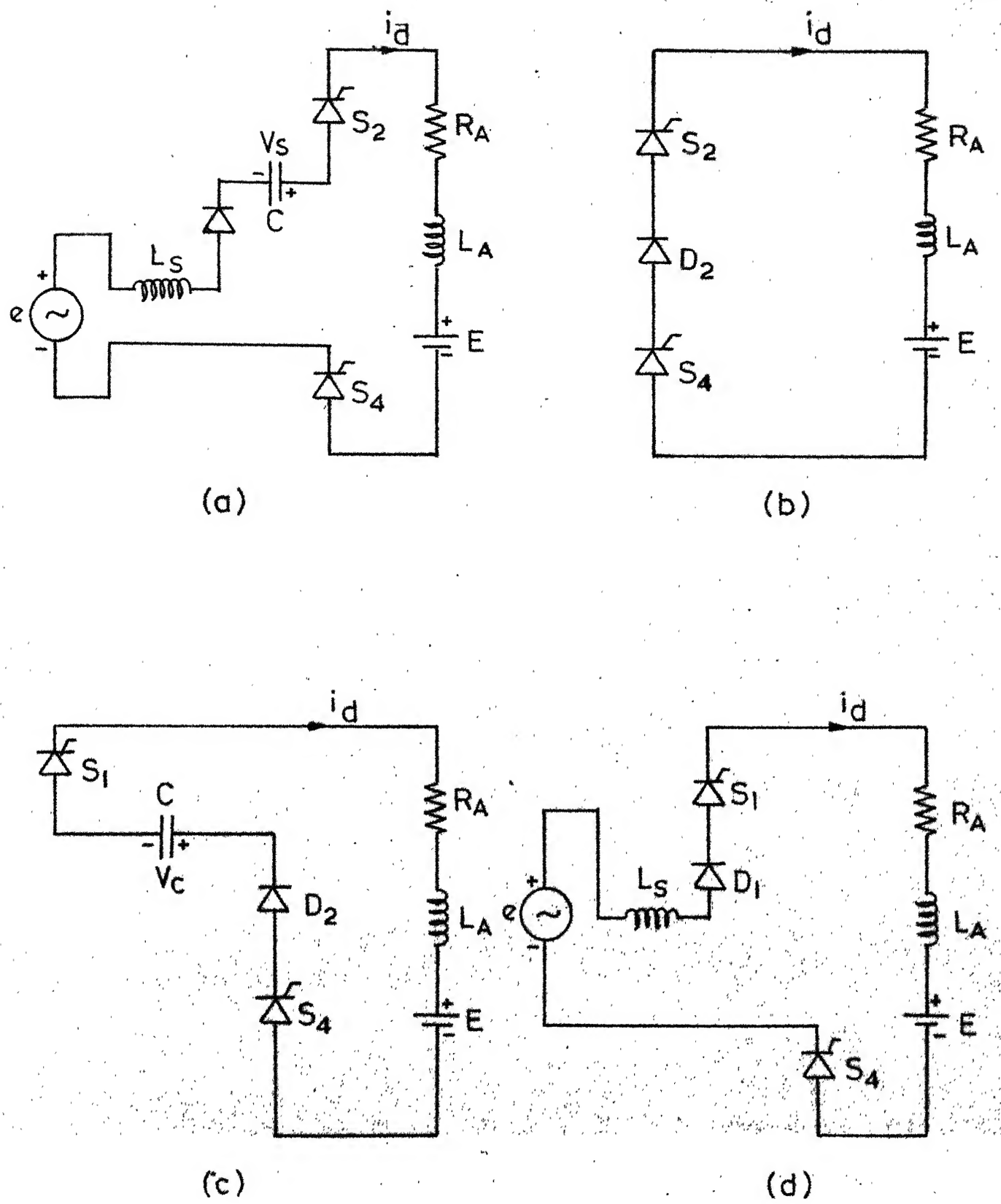


FIG. 4.3.3. VARIOUS POSSIBLE LOOPS FOR STATE VARIABLE Z_3

(b) Applying KCL to Fig. 4.3.4(b) at node B we get

$i_c = i_{L_2} + i_d$ if $S(1) = S(4) = D(2)$ and $D_L(2) = 1$ here

$D(1)$ may also be one alongwith $D(2) = 1$, but not alone. (4.16)

$$C\dot{Z}_4 = Z_3\, S(1)\, S(4)\, D(2) + Z_2\, D_L(2) \tag{4.17}$$

(c) Applying KCL to Fig. 4.3.4(c) at node E, we get

$$i_c = i_{D_2} + Z_2 = C\,\dot{Z}_4 \text{ if } S(1) = S(4) = D(1) = D(2) = 1 \tag{4.18}$$

$$\dot{Z}_4 = \frac{1}{C}\,(i_{D_2}\, S(1)\, S(4)\, D(1)\, D(2) + Z_2\, D_L(2)) \tag{4.19}$$

(d) Applying KCL to Fig. 4.3.4(d) at node D we get

$$i_c = -(i_{D_1} + Z_1) = C\,\dot{Z}_4 \text{ if } S(2) = S(4) = D(1) = D(2) = 1 \tag{4.20}$$

$$\dot{Z}_4 = -\frac{1}{C}\,(Z_1\, D_L(1) + i_{D_1}\, S(2)\, S(4)\, D(1)\, D(2)) \tag{4.21}$$

Combining equations (4.15),(4.17),(4.19),(4.21) and simplifying we get,

$$\dot{Z}_4 = S(4)\,[-(Z_3 + i_{D_1}\, D(2))\, D(1)\, S(2) + (Z_3 + i_{D_2}\, D(1))\cdot S(1)\, D(2)] - Z_1 D_L(1) + Z_2\, D_L(2)\,/C \tag{4.22}$$

4.3.5 Calculation of $\dot{Z}_5$

During the period when both diodes D_1 and D_2 conduct, the load current i_d is assumed to be constant. The currents satisfy the equation

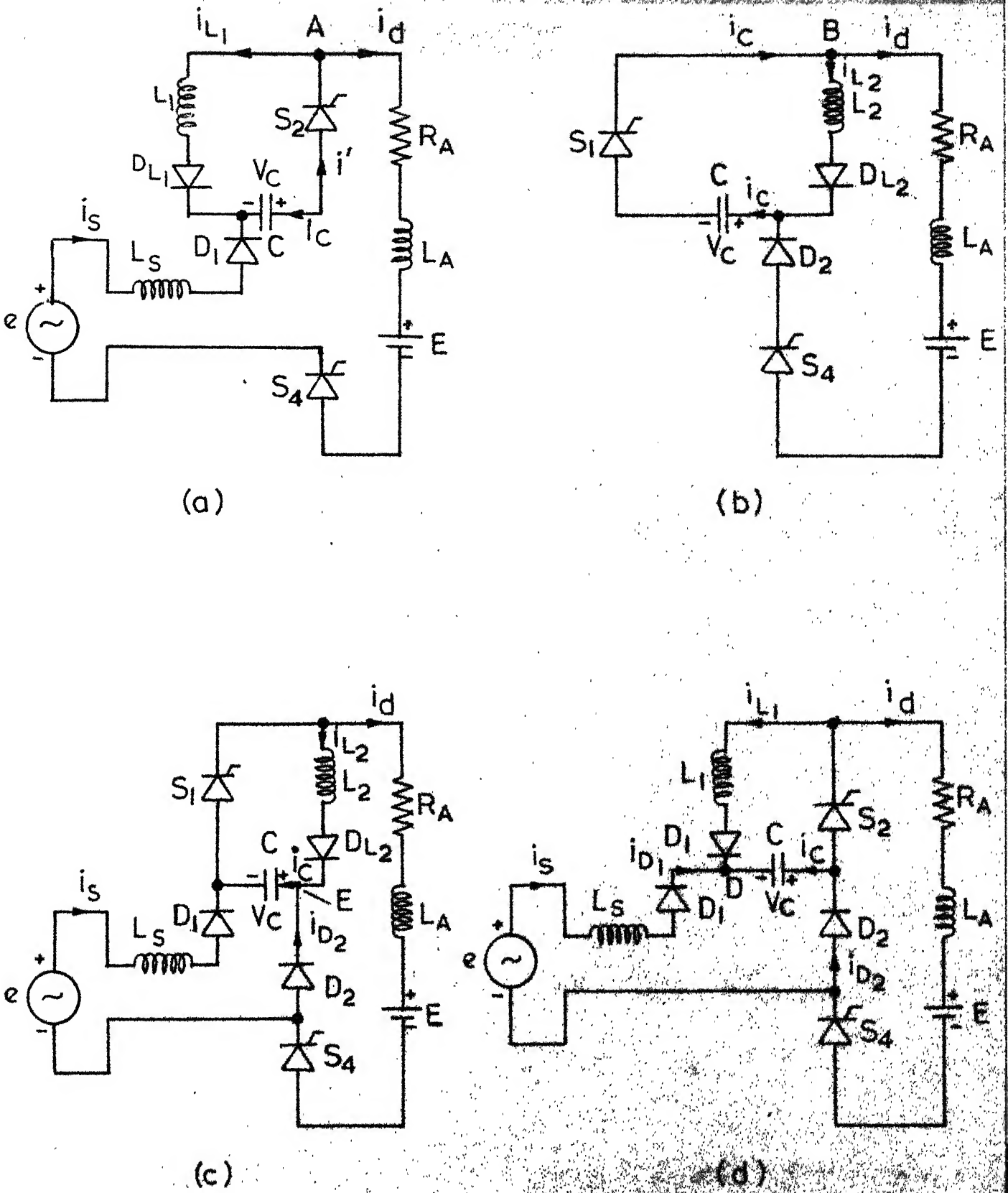


FIG. 4.3.4 VARIOUS POSSIBLE LOOPS FOR STATE VARIABLE Z_4

$$i_d = i_s + i_{\text{diode 2}} \quad \text{at node F}$$

i.e. $Z_3 = Z_5 + i_{\text{diode 2}}$.

The various possible loops are shown in Fig. 4.3.5.

(a) Applying KCL to Fig. 4.3.5(a) at node F we get

$$i_d = i_s + i_{D_2} \quad \text{if} \quad D(1) = D(2) = S(1) = S(4) = 1 \tag{4.23}$$

$$Z_3 = (Z_5 + i_{D_2})\, D(1)\, D(2)\, S(1)\, S(4) \tag{4.24}$$

Now as soon as D_1 starts conducting, with D_2 already conducting, the voltage, $E_m \sin wt + V_c$ will appear across source inductance L_s.

Hence,

$$V_c + E_m \sin wt = L_s \frac{di_5}{dt} = L_s \dot{Z}_5 \quad \text{if } D(1) = D(2) = S(1) = S(4) = 1 \tag{4.25}$$

$$\dot{Z}_5 = \frac{1}{L_S} [E_m \sin wt + V_c] D(1)\, D(2)\, S(1)\, S(4) \tag{4.26}$$

(b) Applying KCL to Fig. 4.3.5(b) at node F we get

$$i_d = i_s + i_{D_2} \quad \text{if } D(1) = D(2) = S(2) = S(4) = 1 \tag{4.27}$$

$$Z_3 = (Z_5 + i_{D_2})\, D(1)\, D(2)\, S(2)\, S(4) \tag{4.28}$$

Now as soon as D_2 starts conducting, with D_1 already conducting, the voltage ($E_m \sin wt + V_c$) will appear across source inductance L_s.

Hence, $Z_4 + E_m \sin wt = L_s \dot{Z}_5$

$$\text{if } D(1) = D(2) = S(2) = S(4) = 1 \tag{4.29}$$

$$\dot{Z}_5 = \frac{1}{L_s} [E_m \sin wt + Z_4] D(1)\ D(2)\ S(2)\ S(4) \tag{4.30}$$

Combining eqns. (4.26) and (4.30) and simplifying we get,

$$\dot{Z}_5 = \frac{1}{L_s} D(1)\ D(2)\ S(4)[(E_m \sin wt + Z_4) S(1) + (E_m \sin wt + Z_4)\ S(2)] \tag{4.31}$$

Also,

$$Z_5 = 0 \quad \text{if} \quad S(2) = D(2) = S(4) = 1$$

$$\text{or} \quad S(1) = S(4) = D(2) = 1 \tag{4.32}$$

$$Z_5 = Z_3 \quad \text{if} \quad S(1) = S(4) = D(1) = 1$$

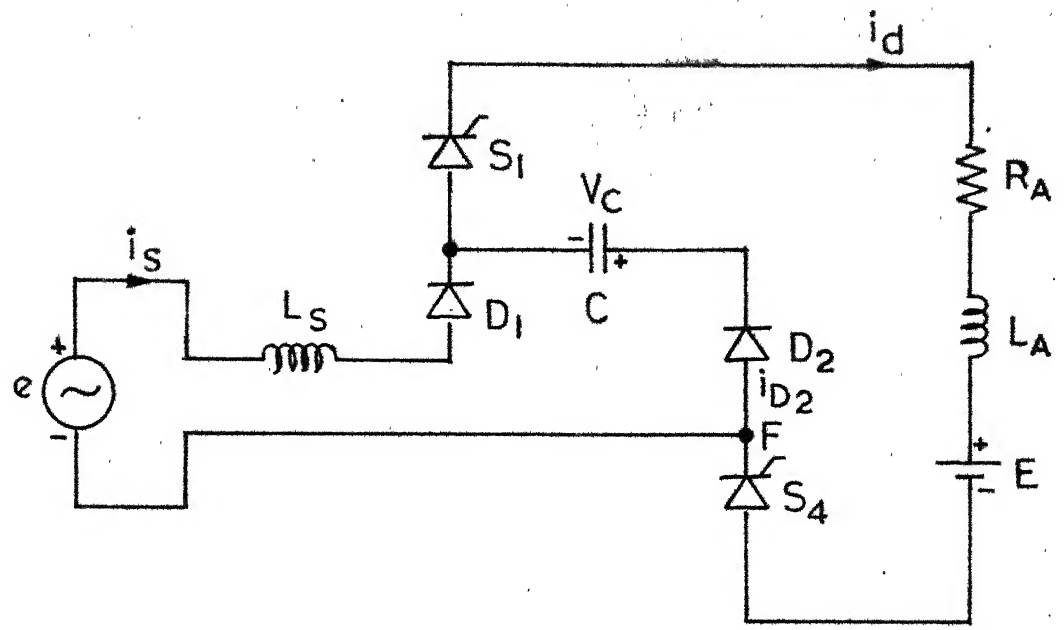
$$\text{or} \quad S(2) = S(4) = D(1) = 1 \tag{4.33}$$

Equations (4.2), (4.4), (4.13), (4.22) and (4.31) are the generalized state equations for the converter circuit of Fig. 4.3.

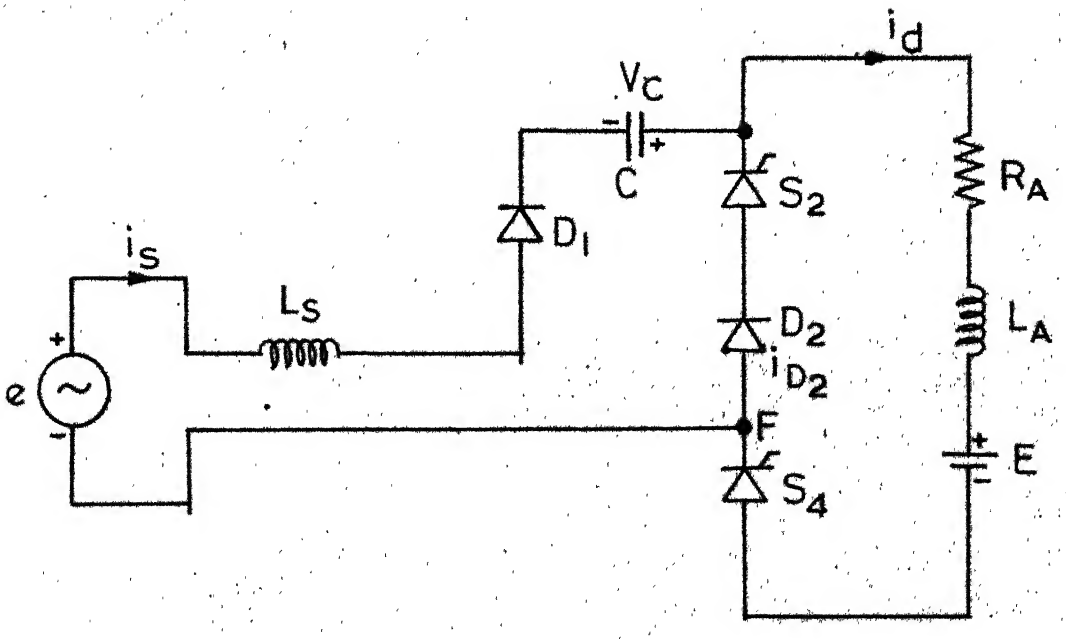
For finding the mode changeover points the values of the logic variables for the devices are to be known. The following equations for the OFF state voltages and the ON state currents are utilized.

4.4 OFF STATE VOLTAGES

From Fig. 4.3 the expressions for the device OFF state voltages can be seen to be :



(a)



(b)

FIG. 4.3.5. VARIOUS POSSIBLE LOOPS FOR STATE VARIABLE Z_5

$$V_{D_{L_1}} = -V_{S_1} \tag{4.34}$$

$$V_{D_{L_2}} = -V_{S_2} \tag{4.35}$$

$$V_{S_2} = (Z_4 + V_S)\ S(1) \tag{4.36}$$

$$V_{S_1} = (V_S - Z_4) \cdot S(2) \tag{4.37}$$

$$V_{S_3} = (V_S - E_m \sin wt) \cdot S(4) \tag{4.38}$$

$$V_{S_4} = (V_S + E_m \sin wt)\ S(3) \tag{4.39}$$

$$V_{D_1} = (Z_4 + V_D + E_m \sin wt)\ D(2) \tag{4.40}$$

$$V_{D_2} = (V_D - Z_4 - E_m \sin wt)\ D(1) \tag{4.41}$$

4.5 ON STATE CURRENTS

From Fig. 4.3 ,the expressions for the device ON state currents can be seen to be :

$$i_{D_{L_1}} = Z_1\ D_L(1) \tag{4.42}$$

$$i_{D_{L_2}} = Z_2\ D_L(2) \tag{4.43}$$

$$i_{S_1} = S(1)\ S(4)\ (Z_3 + Z_2\ D_L(2)) \tag{4.44}$$

$$i_{S_2} = S(2)\ S(4)\ (Z_3 + Z_1\ D_L(1)) \tag{4.45}$$

$$i_{S_4} = Z_3\ S(4) \tag{4.46}$$

$$i_{D_1} = Z_3\ D(1)\ (D(1) - D(2)) \tag{4.47}$$

$$i_{D_2} = Z_3\ D(2)\ (D(2) - D(1)) \tag{4.48}$$

4.6 DIGITAL SIMULATION

The generalized state equations (4.2), (4.4), (4.13), (4.22) and (4.31) are digitally computed to get the different modes of operation and also to obtain the steady-state speed-torque characteristics of a separately excited dc motor.

The flow chart of Fig. 4.4 illustrates the digital solution for motor load. Load torque is assumed initially. To start with, an initial mode is selected. The device currents and state variables are initialized. Binary values are assigned to the device logic variables at instant t=0 secs. For the assumed values of load torque, the values of state variables, device currents and device voltages are computed. The step length is increased and the above computations continued till t = T/2 (half cycle of input line frequency). Now the convergence of the state variables and the load current is checked. If any one of them has not converged then the corresponding initial values are corrected and the iterations are continued. This process is continued till all the state variables and load current converge. The steady state speed is calculated.

Also the instantaneous values of the state variables are found out indicating the mode changeover points. Hence, the solution is obtained by an iterative procedure.

The program, written in FORTRAN IV . has been

successfully run on DEC-1090 system. A listing of the program and a sample output for motor load is given in Appendix II-A and II-B respectively.

4.6.1 Motor load

The simulation was carried out for a separately excited dc motor. The lumped circuit model for the motor was adopted (Appendix I). The converter-motor is simulated for only continuous conduction as the range of discontinuous current conduction is much less for a forced commutated converter,feeding a separately excited motor (Chapter 3). The flow chart of Fig. 4.4 is used to obtain the simulation results for a motor load.

Variation for state variables i_d,i_s,V_c,$i_{D_{L_1}}$,$i_{D_{L_2}}$ and output voltage v_d and voltage across SCR S_1,$V_s$for one half cycle in the steady state are shown in Fig. 4.5.

From the plot of the output voltage it can be seen that when SCR S_1 is switched ON to take over from SCR S_2 (i.e. power interval to the freewheeling interval)there is a positive voltage spike, which occurs because capacitor voltage gets added to the input voltage. This spike occurs for a very short duration (depending on the LC resonant time) as the reversal of capacitor charge is load independent. When the SCRS, is turned ON to commutate the SCR S_2,a positive spike occurs (capacitor voltage appearing across load). The

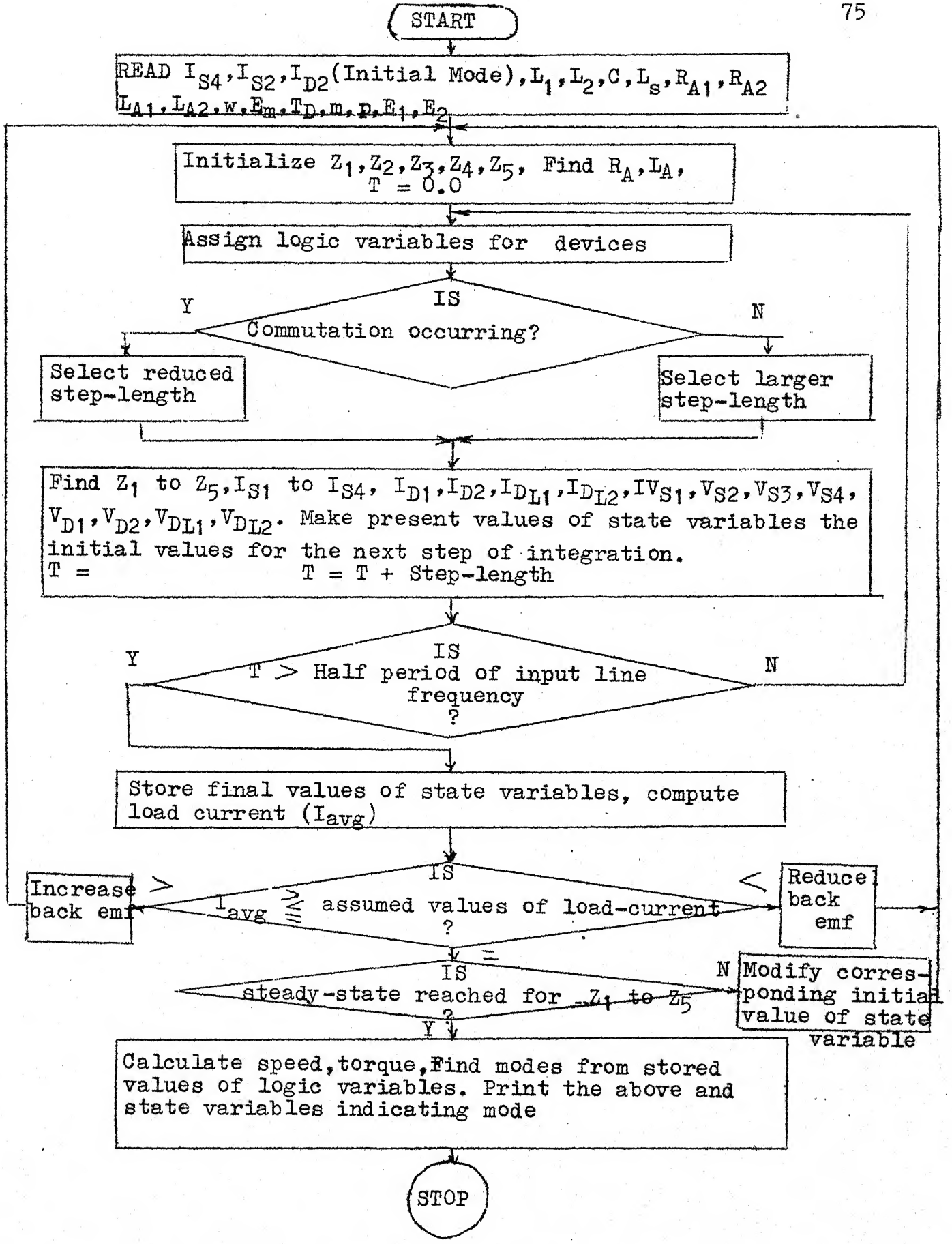


Fig. 4.4 Flow Chart for Analysis of Circuit of Fig. 4.3 with Motor Load

output voltage continues to follow the capacitor voltage and goes negative. This is because both D_1 and D_2 conduct simultaneously during this period and since the LC resonant time period is less than the time required for D_2 to turn-off. The negative spike does not appear in the case of second, third and fourth pulses. This can be attributed to the fact that since the rate of fall of current in D_1 is proportional to the line voltage E_m sin wt and since for these pulses the line voltage is higher than for pulses 1 and 5, the current in diode D_2 falls to zero faster than L C resonant time period and there is no occurrence of negative spike. For the same reason as above the spike is less in fifth pulse as compared to first pulse. The output current continuously increases during the power interval for about four pulses. Since the curves are presented for the motor load having low $Q_L (= 3.14)$, they are far from an ideal flat topped one.

The various modes which occurred over the half cycle are shown in Table I.

The various sequence of modes during five pulses followed by the freewheeling interval are shown in Table II.

The simulation for an RL load with the same load current, commutation parameters, input source inductance and line frequency was carried out. Fig. 4.6 shows the variation in the capacitor voltage and output voltage over a period of

TABLE I

operating modes during one half-cycle (+ve)

X : Indicates conducting device

Mode	Devices Conducting							
	S_1	S_2	S_3	S_4	D_1	D_2	D_{L_1}	D_{L_2}
1	X			X		X		X
2	X			X	X	X		X
3	X			X	X			X
4	X			X	X			
5		X		X	X		X	
6		X		X	X	X	X	
7		X		X		X	X	
8		X		X		X		
9		X		X	X			
10		X		X	X	X		

TABLE II

Sequence of modes during +ve half-cycle

Pulse	Sequence of Modes	Sequence
1	1-2-3-4-5-6-7-8	A
2	1-2-3-4-5-9-10-8	B
3	1-2-3-4-5-6-10-8	C
4	1-2-3-4-5-6-10-8	C
5	1-2-3-4-5-6-7-8	A

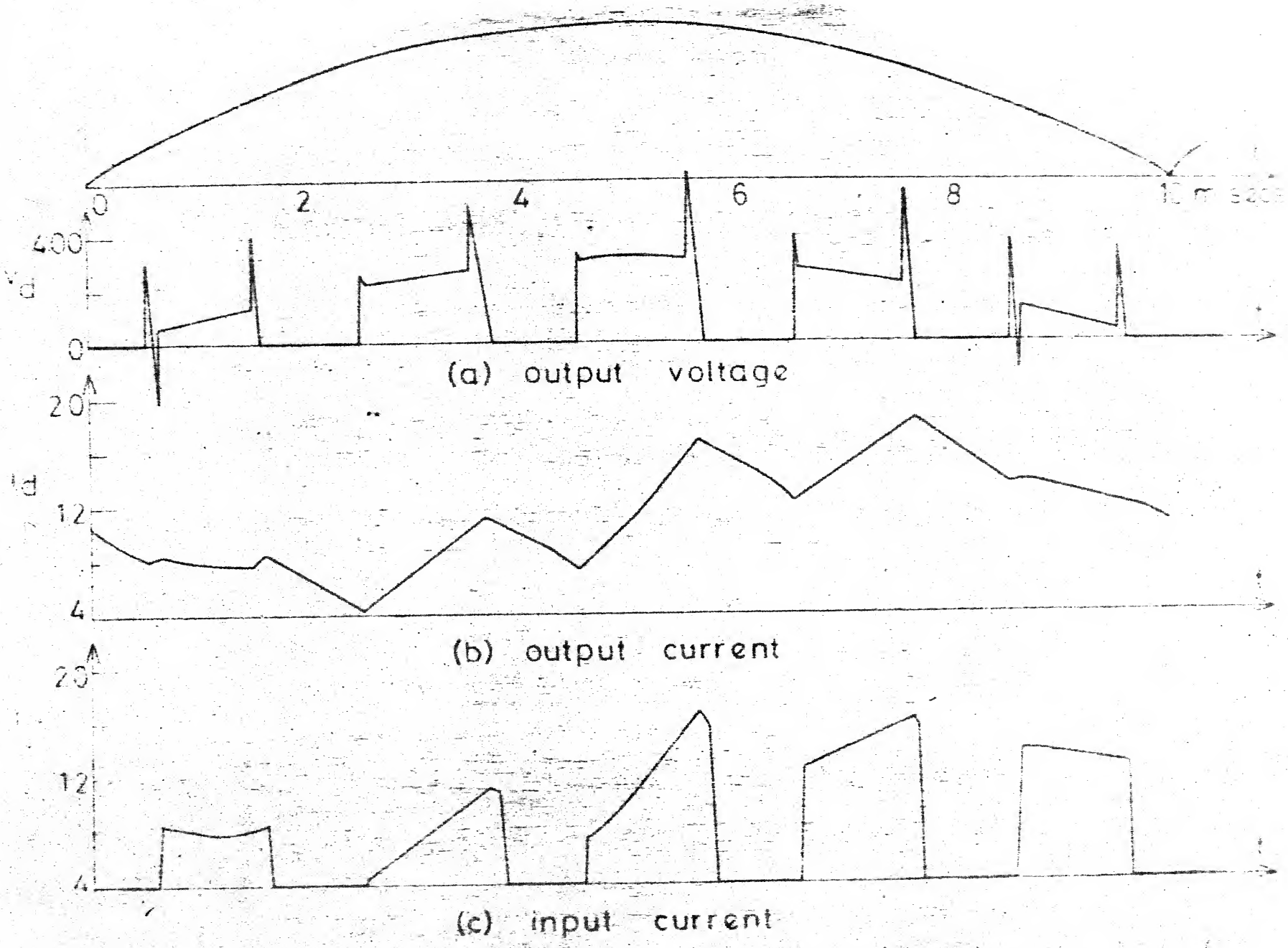
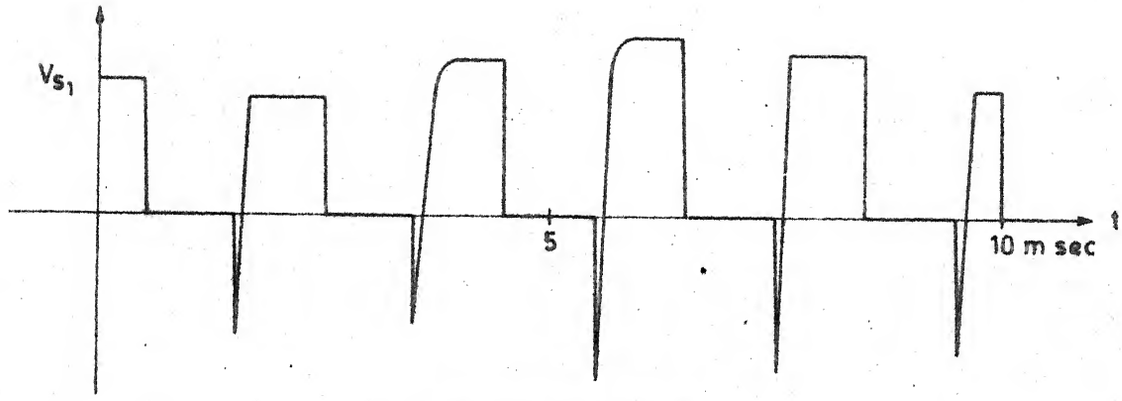

0
2
4
6
8
400
0
(a) output voltage
20
12
4
(b) output current
20
12
4
(c) input current

Fig. 4.5 (contd.)



(d) Voltage across S_1

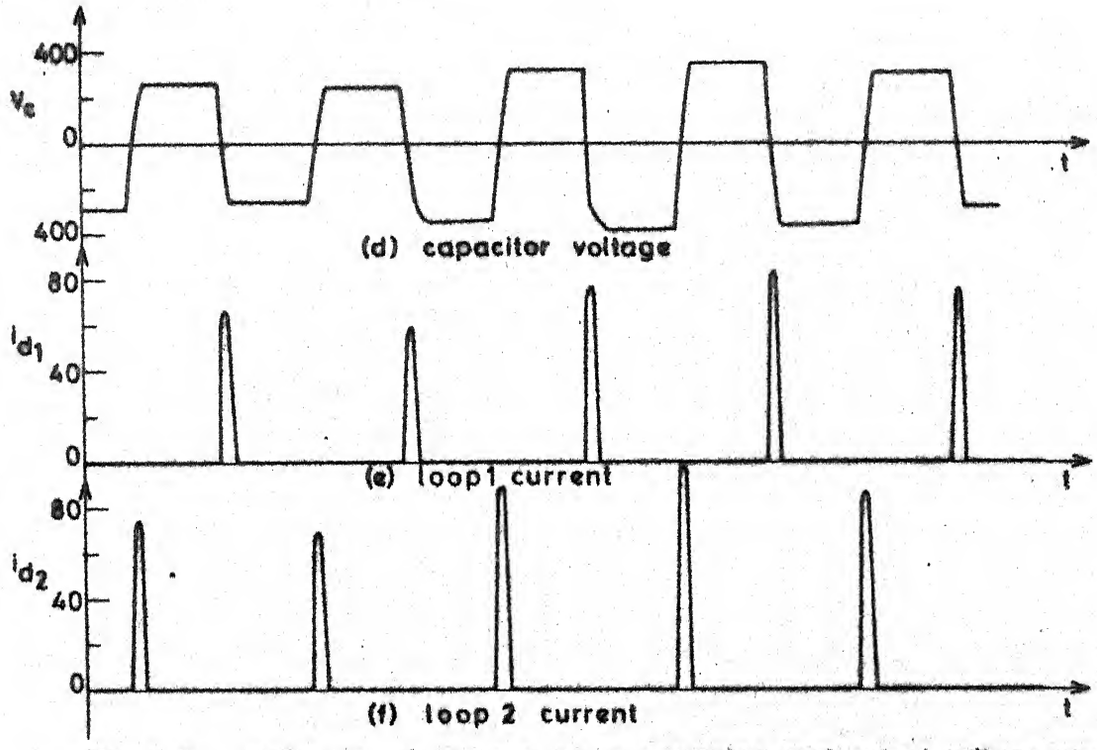


Fig. 4.5 Variation of various state variables and output voltage over half cycle for motor load. $L_1 = L_2 = 192\,\mu H$, $C = 15\,\mu fd$, $L_s = 390\,\mu H$, $m = 0.5$, $p = 5$.

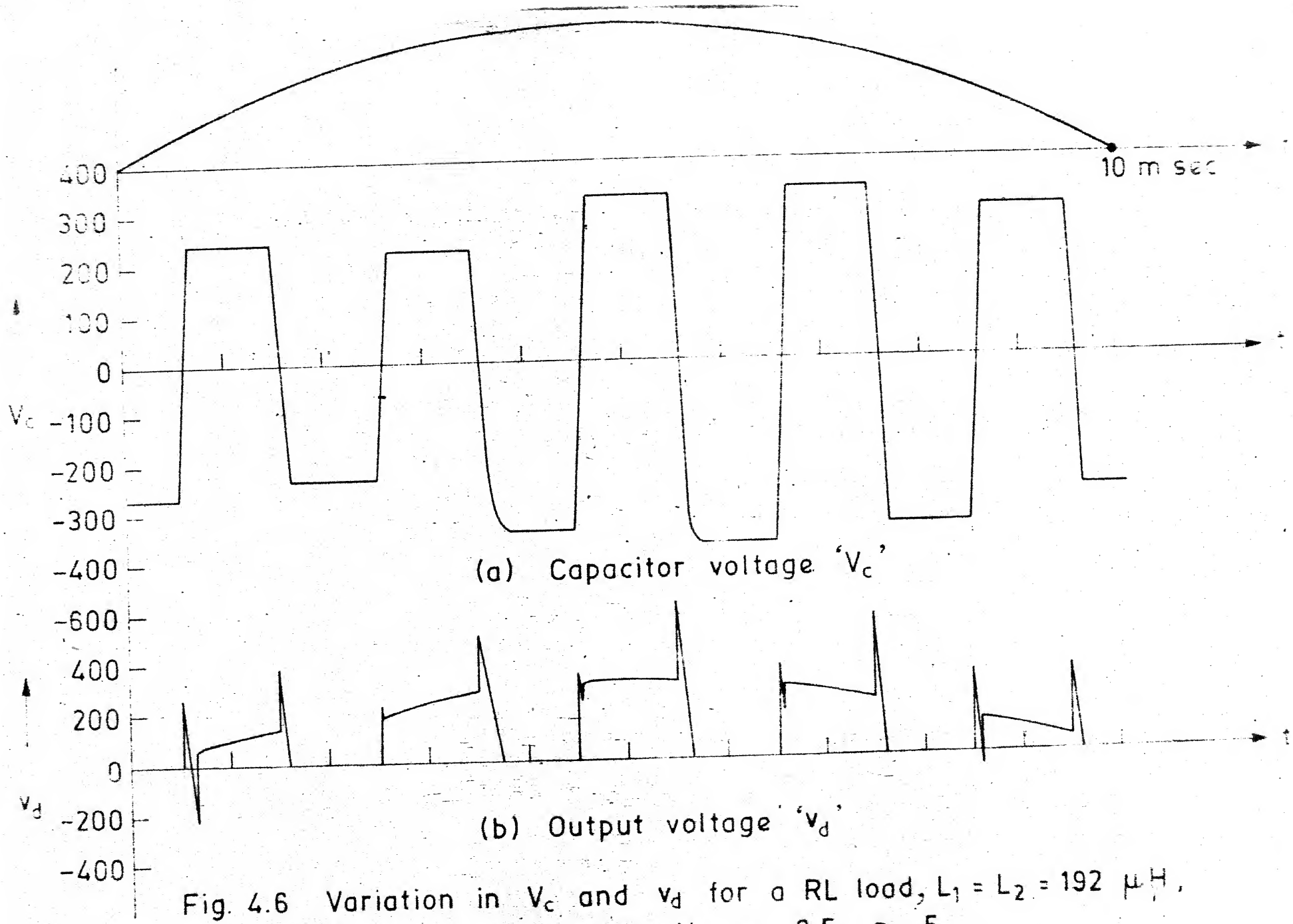


Fig. 4.6 Variation in V_c and v_d for a RL load, $L_1 = L_2 = 192\ \mu H$, $C = 15\ \mu fd$, $L_s = 0.39$ mH, $m = 0.5$, $p = 5$.

half cycle. Comparing these waveforms with the corresponding waveforms for motor load (Fig. 4.5), it may be concluded that there is no difference in the circuit behaviour with R-L and motor load. The mode sequence for the five pulses were found to be the same as in Table II.

For lower values of LC resonant time, a sequence D (1-2-11-4-5-6-7-8) was found to occur for the first pulse and fifth pulse. The change is quite obvious for the LC resonant time has been reduced and hence D_1 and D_2 conduct for a time greater than one half LC resonant time at reduced line voltage. During mode 11, the active devices conducting are S_1, S_4, D_1 and D_2.

4.7 CIRCUIT BEHAVIOUR

The circuit behaviour during the four possible sequences is explained below :

4.7.1 Sequence A

The commutation transients occuring are shown in Fig. 4.7(a).

Initially S_2, S_4 and D_2 are conducting (Mode 8). When S_1 is triggered (instant $t = t_o$), the capacitor starts charging through the loop $S_1 - D_{L_2} - L_2 - C$ and also the load current starts charging the capacitor through the loop S_1 - Load - S_4 - D_2 - C - S_1. The output voltage at this instant jumps to capacitor voltage (Mode 1). At

instant $t = t_1$ the capacitor charges upto the line and hence D_1 starts conducting. The input line current i_s starts building up slowly at the rate governed by $\frac{dis}{dt} = \frac{1}{L_s}$ (E_m sin wt + V_c). For the same reason i_{D_2} starts falling slowly. During this period $i_{D_2} + i_S = i_d$. The output voltage still follows the capacitor voltage (Mode 2). At instant $t = t_2$, i_{D_2} falls down to zero and hence D_2 stops conducting. The capacitor continues to charge through the path C - S_1 - D_{L_2} - L_2. The output voltage jumps to the line voltage and starts following it (Mode 3). At instant $t = t_3$, $i_{D_{L_1}}$ goes down to zero. The transients end and the normal load cycle starts (Mode 4). The active devices conducting here are S_1, D_1 and S_4.

Now when S_2 is triggered (at $t = t_o'$), the capacitor starts discharging through the path C - D_{L_1} - D_1 - S_2 and e - D_1 - C - S_2 - load - S_4. The output voltage jumps to (E_m sin wt_o' + V_c) and falls as the capacitor discharges (Mode 5). At instant $t = t_1'$, the capacitor discharges to the line voltage and hence D_2 starts conducting. Line current i_s starts falling at the rate governed by, $\frac{di_s}{dt} = \frac{1}{L_s}$ (E_m sin wt + V_c). Current i_{D_2} starts building up. The capacitor continues charging up in the other direction (Mode 6). At $t = t_2'$, i_s falls down to zero. The load current starts freewheeling through S_2-D_2-S_4. The output voltage falls down to zero. The capacitor is still charging through the path S_2 - D_{L_1} - L_1 - C (Mode 7). At instant $t = t_3'$, $i_{D_{L_1}}$ falls down to zero. Mode 8 begins.

4.7.2 Sequence B

The commutation transients occuring are shown in Fig. 4.7(b).

When switching from S_2 to S_1 modes are same as for sequence A.

When switching is done from S_1 to S_2, mode 5 follows mode 4 (explained earlier). At instant $t = t_1'$, $i_{D_{L_1}}$ falls down to zero but the capacitor charge is still less than the line voltage and hence D_2 does not pick up conduction. The capacitor continues to charge in the negative direction through the path S_2 - load - S_4-e-D_1-C (Mode 9). At instant $t = t_2'$, the capacitor voltage becomes equal to line voltage and hence D_2 starts conducting. Currents i_s starts falling. During this period, overcharging of capacitor in the negative direction occurs. Output voltage is zero (Mode 10). At instant $t = t_3'$, i_s falls down to zero. Mode 8 follows.

4.7.3 Sequence C

The commutation transients occuring are shown in Fig. 4.7(c).

When switching is done from S_2 to S_1, the modes remain the same as for sequence A.

When switching is done from S_1 to S_2, modes 5 and 6 follow mode 4 (explained earlier). At instant $t = t_2'$, $i_{D_{L_1}}$

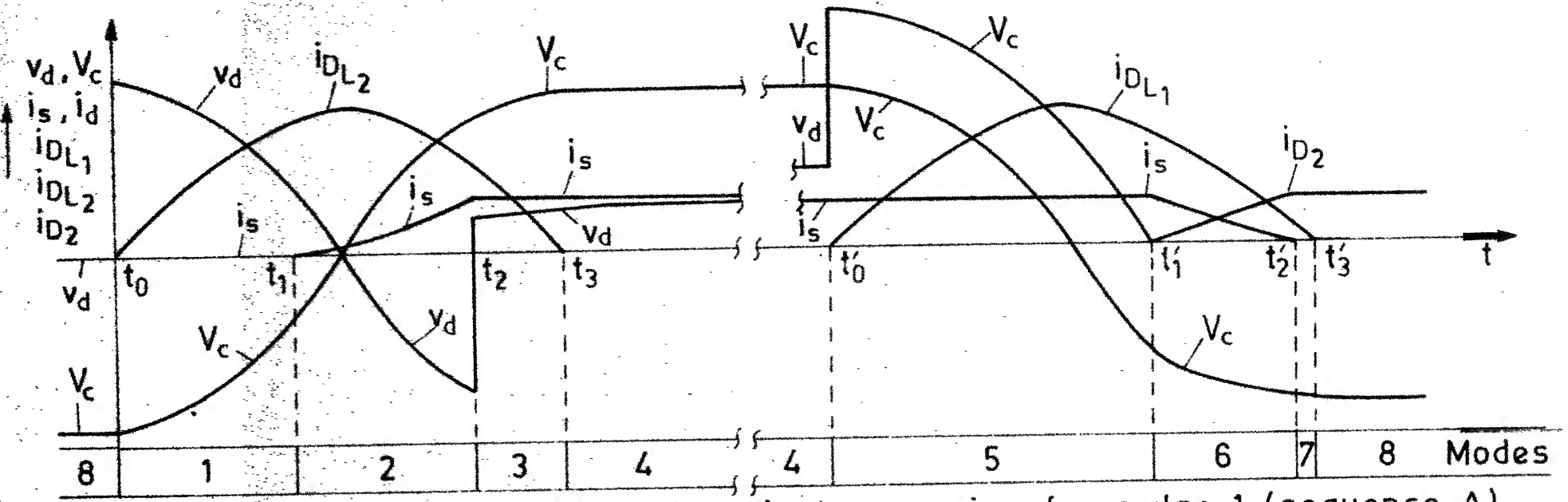


Fig. 4.7 (a) Typical commutation transients occuring for pulse 1 (sequence A).

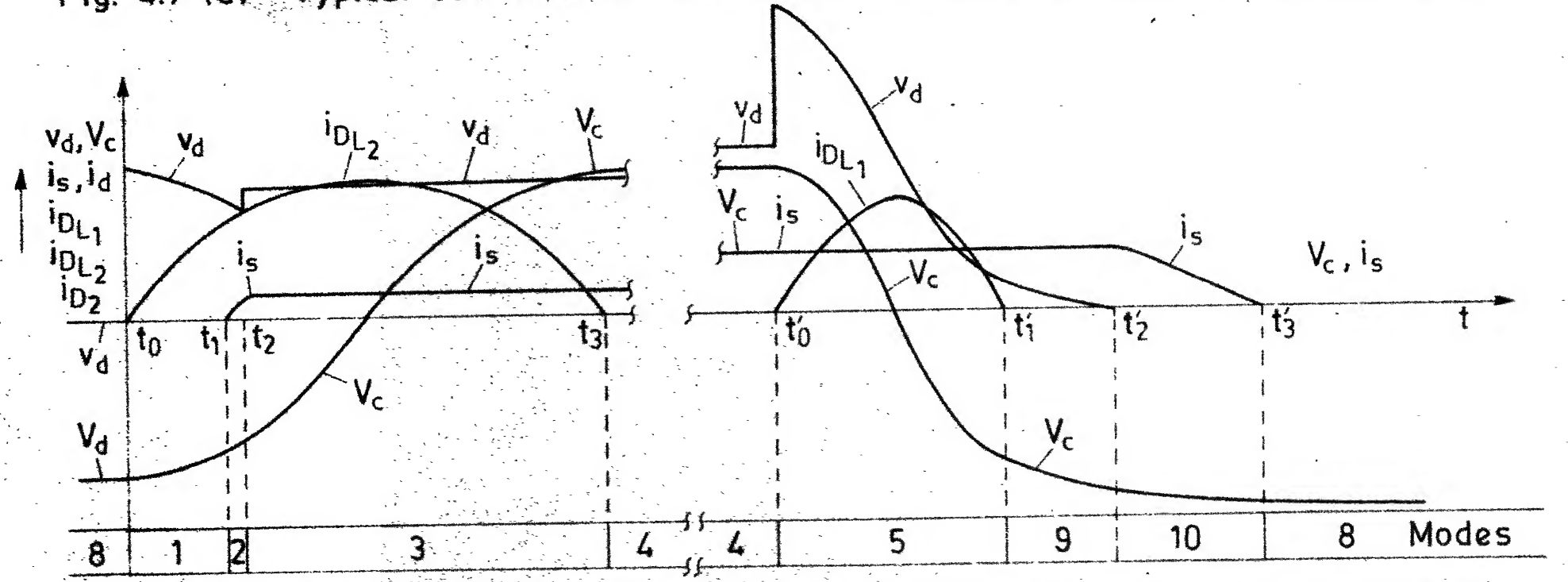


Fig. 4.7 (b) Typical commutation transients occuring for pulse 2 (sequence B)

goes down to zero, D_1 and D_2 continue to conduct. Current i_s continuously falls, while i_{D_2} steadily increases. Capacitor continues to overcharge in the negative direction (Mode 10). At instant $t = t_3'$, i_s falls down to zero and freewheeling starts (Mode 8).

4.7.4 Sequence D

The commutation transients occuring are shown in Fig. 4.7(d).

When switching from S_2 to S_1, modes 1 and 2 follow mode 8 (explained earlier). At instant $t = t_2$, $i_{D_{L_2}}$ goes down to zero. D_1 and D_2 continue to conduct and the capacitor overcharges through the path S_1-load-S_4-D_2-C. The output voltage continues to follow the capacitor voltage (Mode 11) and goes negative. At instant $t = t_3$, i_{D_2} falls down to zero. The load cycle begins (Mode 4).

4.8 SPEED-TORQUE CHARACTERISTICS

The flow chart for finding the speed-torque characteristics for both continuous and discontinuous armature current conduction without taking the commutation effect into account is shown in Fig. 4.8. Five pulses are considered. The eddy current model as explained in Appendix I is taken into account while computing the speed-torque characteristics.

The speed-torque characteristics for a separately excited dc motor (the eddy current model constants of which are given in Appendix I) are shown in Fig.4.9(a). From the characteristics we can infer that the speed regulation is very good even in the discontinuous current conduction range.

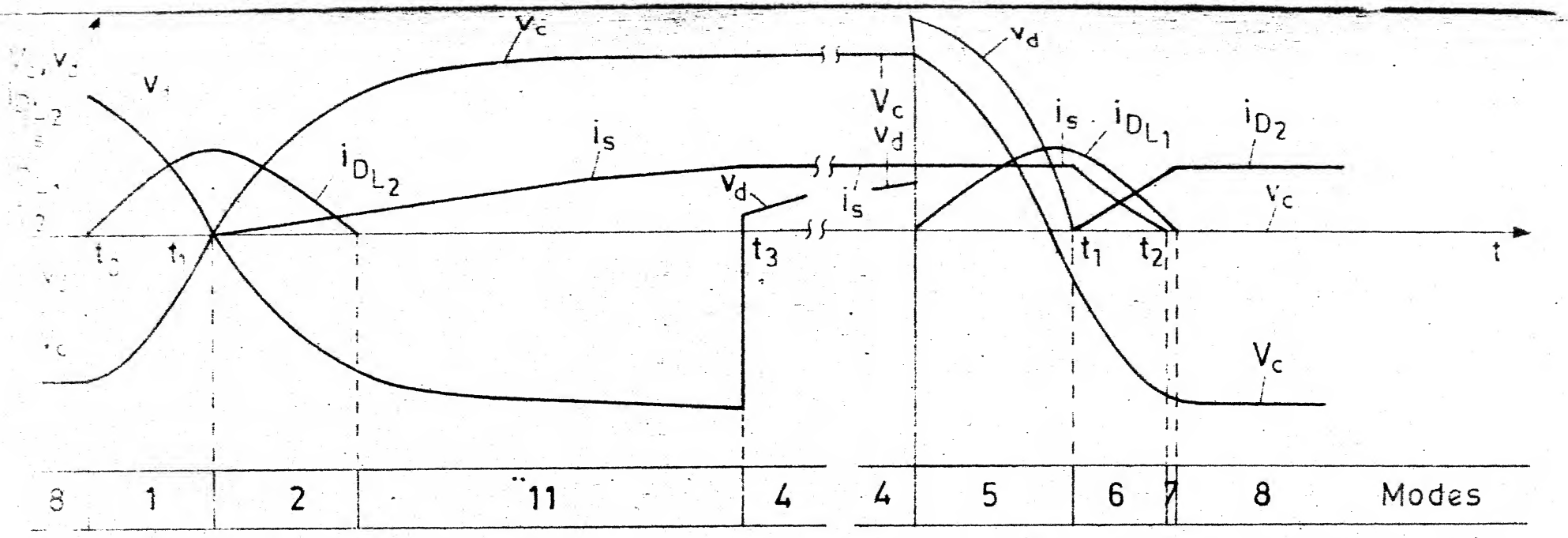


Fig. 4.7(d) Typical commutation transients occuring for pulse 1 (sequence D).

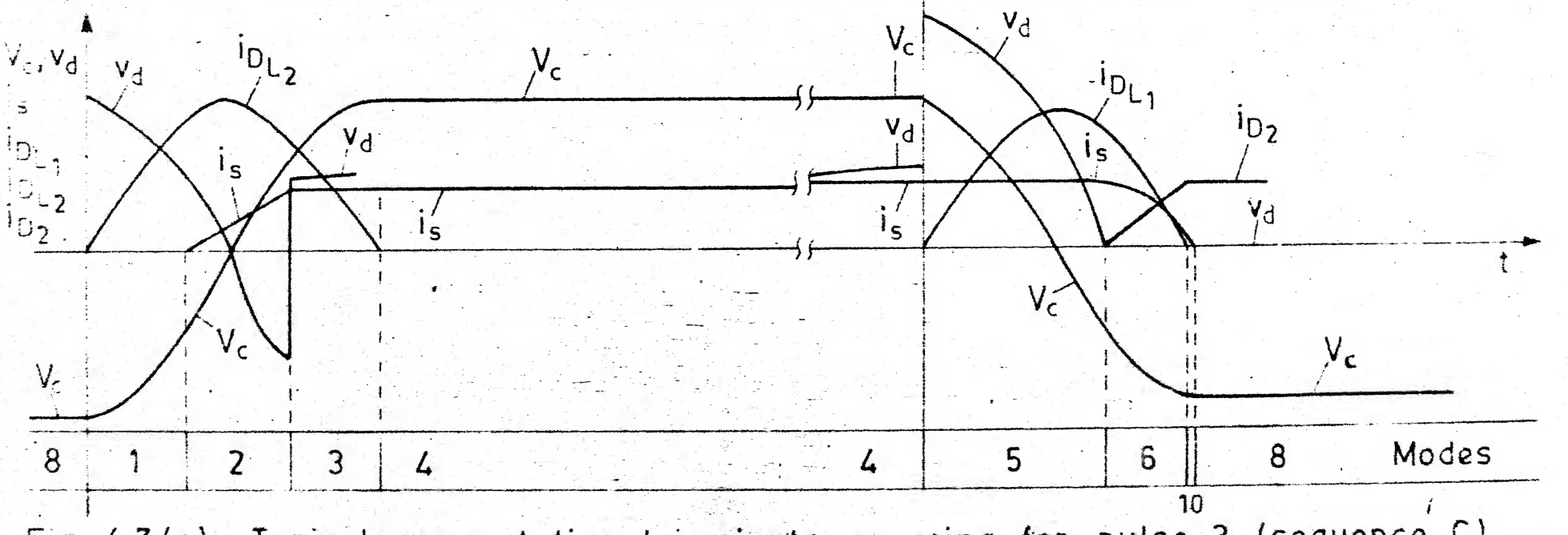


Fig. 4.7(c) Typical commutation transients occuring for pulse 3 (sequence C).

The speed-torque characteristics with and without commutation transients are shown in Fig. 4.9(b). The flow chart of Fig. 4.4 has been considered for getting the speed-torque characteristics taking the commutation transients into account. It is noted that the speed increases over the entire torque range if the commutation transient is taken into consideration. The increase in speed is appreciable for low values of modulation index, but gradually decreases for higher values of modulation index. This is because of the presence of positive voltage spikes during commutation of S_1 and S_2. These spikes increase the average dc output voltage, thereby increasing the speed for a given torque.

The effect of the LC commutation time period on the speed-torque characteristics is shown in Fig. 4.9(c). It can be seen that as the time period is increased, the speed-torque characteristics departs considerably from that without commutation. This is as expected since the spikes span a larger time with increasing commutation time period, thereby causing an increase in the dc output voltage.

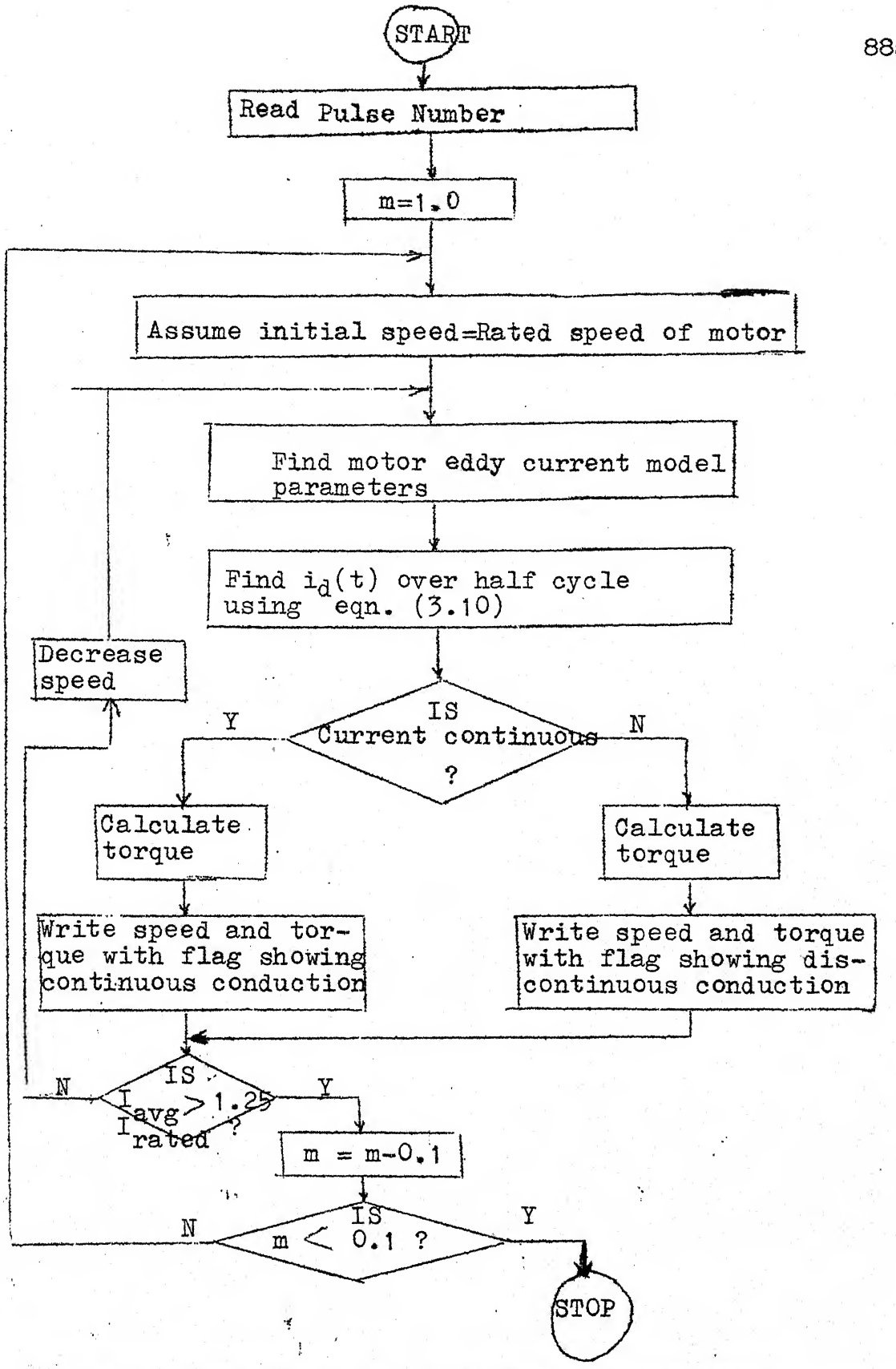


Fig. 4.8 Flow Chart for Finding the Speed Torque Characteristics of Motor without Taking Commutation into Account

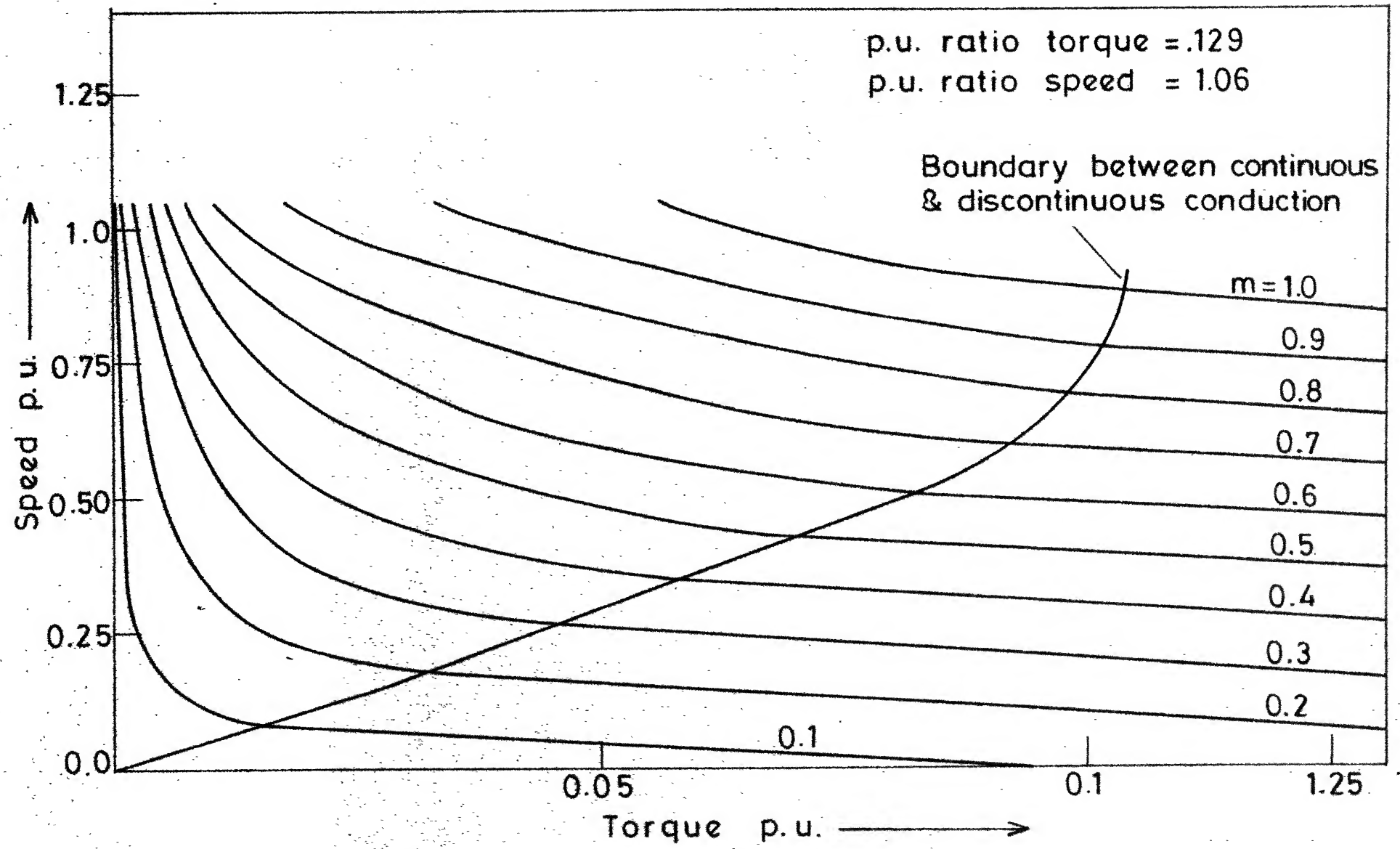


Fig. 4.9(a) Speed-torque characteristics without commutation effect p = 5.

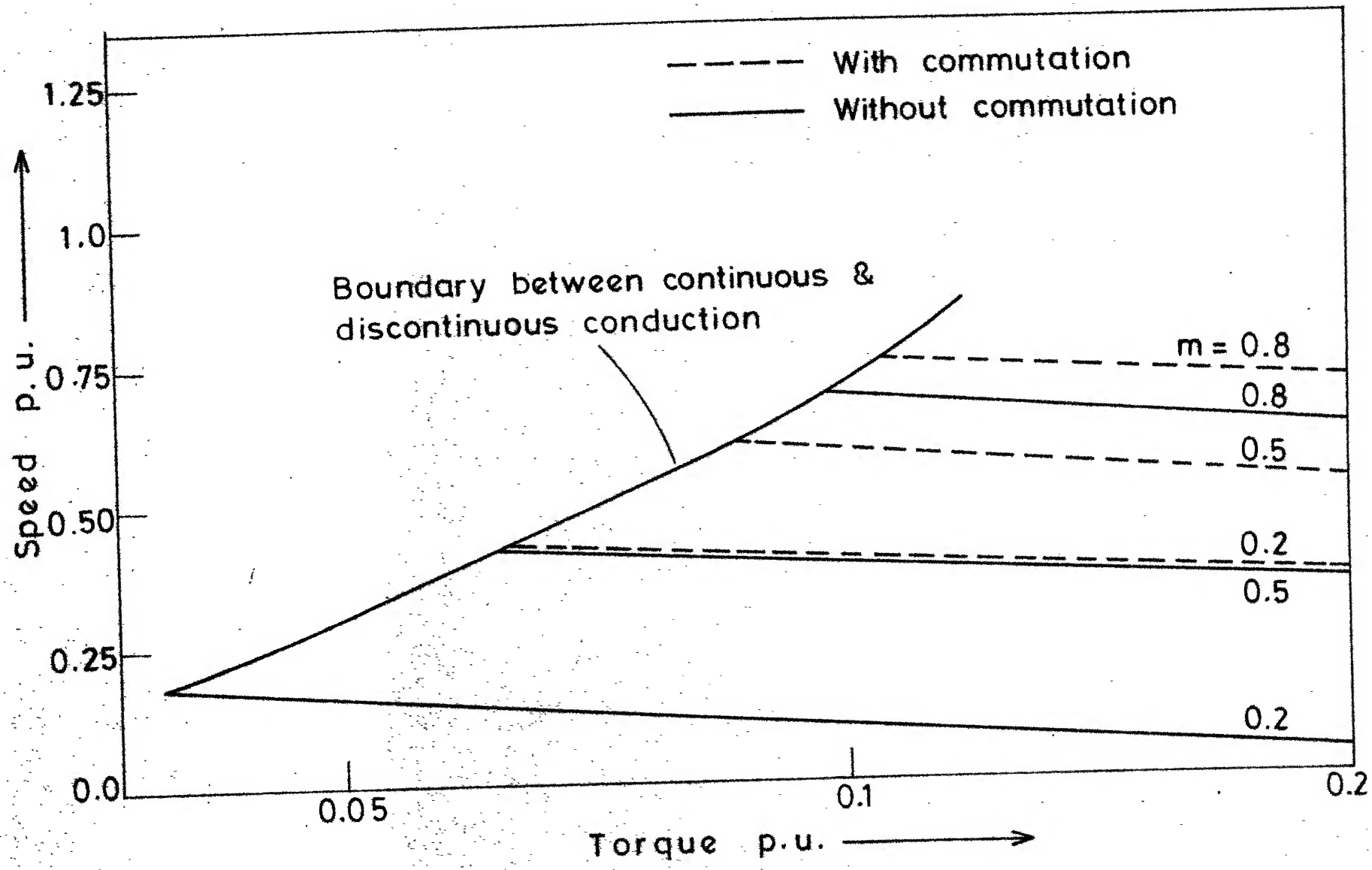


Fig. 4.9(b) Effect of commutation on speed-torque characteristics p = 5.

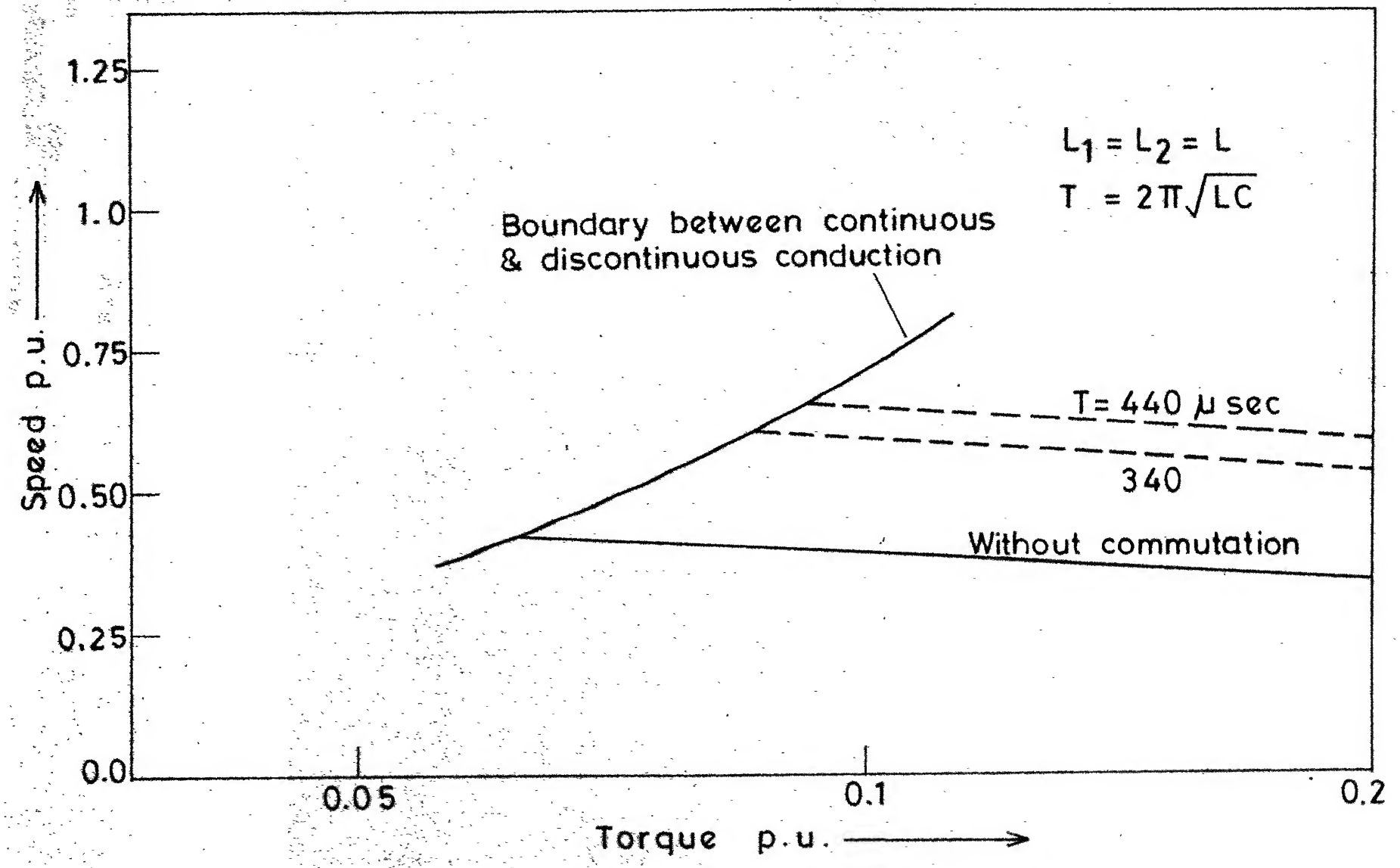


Fig.4.9(c) Effect of LC resonent time on speed-torque $m = 0.5, p = 5$.

4.9 TURN-OFF TIME FOR MAIN SCRs

Fig. 4.10 shows the variation in the turn-off time available for SCRs S_1 and S_2 with the load current. Since the turn-off time is dependent on the position of the pulse, it is shown as a band from the maximum to the minimum value. The curves are plotted for a modulation index of 0.5 and pulse number = 5. It is seen that the 5th pulse has a minimum turn-off time for both S_1 and S_2. Also the turn-off time decreases for increasing load current values. For decreasing loads the turn-off time approaches the ideal value equal to one-quarter of LC resonant period ($\frac{\pi}{2}\sqrt{LC}$).

4.10 CONCLUSIONS

The sequence of modes of a pulse-width modulated ac-dc converter with R-L load and a separately excited motor load are the same provided the armature current is continuous. The negative spikes which occur in the output voltage decrease with increased LC resonant time period, which results in a reduced output voltage variation on the lower values. If we remove the source inductance L_s, the problem of the negative spike is eliminated, but the presence of L_s assures commutation even at lower values of input voltage. With the use of SCRs having low turn-off (= 10 μsec) time, the speed-torque characteristics can be made to correspond more to the one without commutation, also the range of output voltage variation will not decrease as lower values of LC resonant time

can be taken. S_2 has a higher turn-off time available to regain the forward blocking capacity than S_1, this is due to the overcharging of the capacitor (because of the presence of source inductance L_s) when S_2 is conducting. This larger voltage on the capacitor gives a larger turn-off time to S_2 during subsequent firing of S_1.

Experimental verification of simulated results are presented in the next chapter.

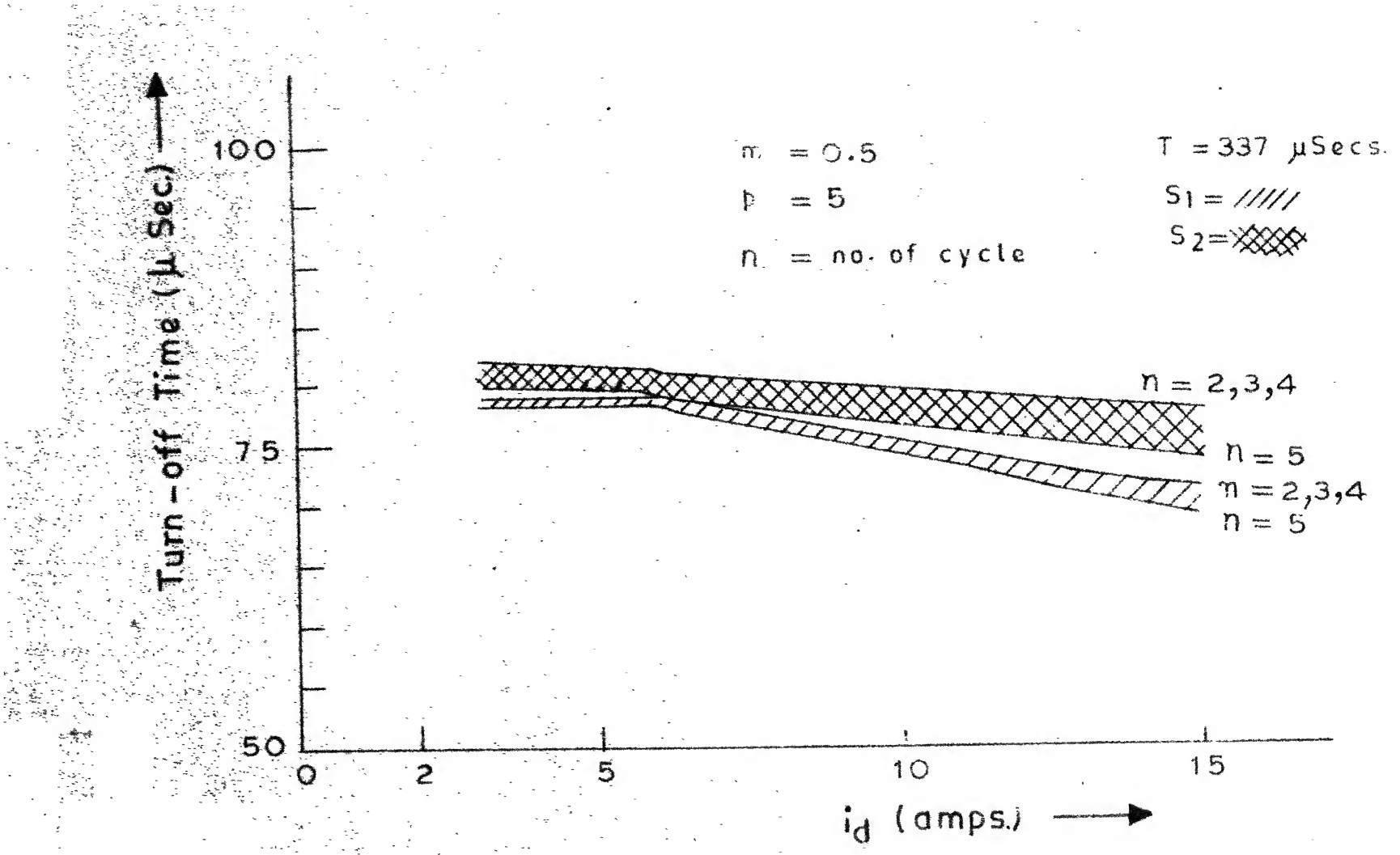


FIG. 4.10 Turn-off time available for SCRs S_1 and S_2

CHAPTER V

CONTROL CIRCUIT DETAILS AND EXPERIMENTAL VERIFICATION OF AC-DC CONVERTER WITH R-L AND MOTOR LOAD

5.1 INTRODUCTION

In the present chapter, a novel firing circuit has been developed for the converter circuit of Fig. 4.3. The triggering strategy is chosen such that the precharging of the commutating capacitor C while starting the converter circuit initially is not required. Most converter circuits which operate on forced commutation do not have such a feature. This is an added advantage for the converter circuit of Fig. 4.3 which is simple and versatile. The effect of switching ON the control circuit at any particular instant on the starting of the converter circuit without precharging of commutating capacitor has been discussed in detail. The control circuit is described in detail. The modifications required for the use of the firing circuit for regenerative operation of the converter has also been discussed. The operation of the converter circuit with both R-L and motor (separately excited DC motor) loads has been studied experimentally with the control circuit developed in this chapter. The experimental results - ac supply power factor, speed-torque characteristics and modes of operation are then compared with the digital simulation results.

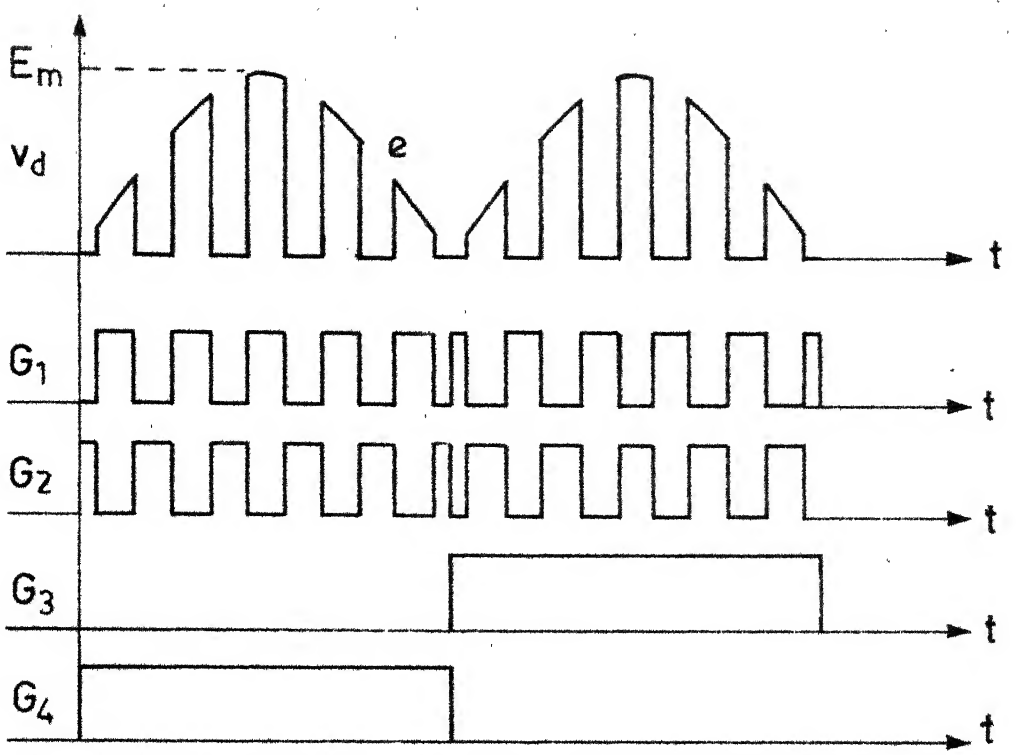


Fig. 5.1 Control signals for SCR$_s$ S_1 through S_4.

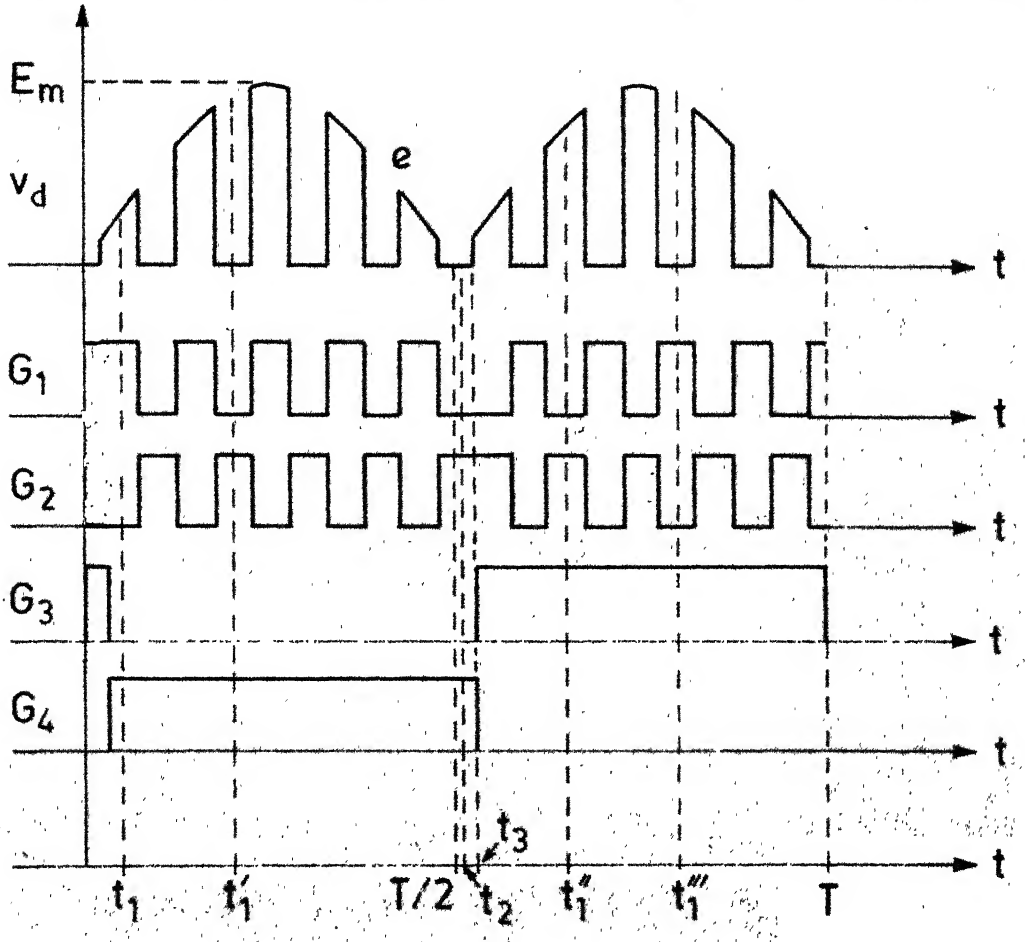


Fig. 5.2 (a) Control signals for SCR S_1 to S_4 for an improved control strategy (Rectification).

5.3.1 Case I

Assume that the control circuit is activated at $t = t_1$ after the line voltage is switched at $t = 0$. From the firing sequence of Fig. 5.2(a), it can be seen that at instant $t = t_1$, the gate pulses for SCRs S_1 and S_4 are present. Since both of them are forward biased they will start conducting. The input line voltage is applied across the load circuit and the load current starts building up through the path e-D_1-S_1-load-S_4. Subsequently, the presence of a gate pulse to SCR S2 will not turn it ON because in the absence of any charge across the capacitor C, it virtually acts as a short and the forward conduction drop of S_1 reverse-biases S_2. Thus S_1, D_1 and S_4 continue to conduct with load current continuously building up. At the instant $t = T/2$, diode D_2 becomes forward biased and starts conducting. Because of the presence of source inductance L_s, the current i_s falls slowly. Currently i_{D_2} starts building up. Thus charging of the capacitor through the path S_4-D_2-C-S_1-load starts taking place in the positive direction(as indicated in Fig. 4.3). The loop S_1-load-S_4-e-D_1-S_1 is still active. At instant $t = t_2$, say, i_s becomes zero and i_{D_2} becomes equal to the load current. At $t = t_2$, the circuit becomes isolated from the source voltage.

Since C is charged up, S_2 will turn ON because the gate signal is already present for S_2 which is forward biased at this instant. The capacitor charge reverses through the loop S_2-L_1-D_{L_1}-C-S_2 and the load current starts freewheeling through S_4, D_2 and S_2. D_{L_1} stops conducting after one half resonant time period ($\pi/\sqrt{L_1 C}$). The load current however continues to freewheel until $t = t_3$ when the gate pulse occurs to S_3, which is forward biased. S_3 turns ON and it turns off S_4 by ac line commutation. Subsequently the occurrence of gate pulses to SCR's S_1 and S_2 provide freewheeling and power intervals since the SCR S_4 is already turned OFF. During these periods the capacitor charges up with appropriate polarity required for commutation.

Thus we see that the delayed application of firing pulse to SCR S_3 ($t = t_3$) helps in charging up of capacitor, without the necessity of precharging before the converter is started.

5.3.2 Case II

We assume that the gate pulses to SCRs S_1 through S_4 are applied at instant $t = t_1'$, after the voltage is switched at $t = 0$. From the firing sequence of Fig. 5.2(a) it can be seen that at instant $t = t_1'$, gate signals for SCRs S_2 and S_4 are present. D_1 and S_4 being forward biased, start conducting. Since capacitor has zero voltage, it acts as a short making S_2 forward biased. S_2 turns ON since the gate pulse is already

present. Load current starts building up.

The capacitor starts charging up with the load current in reverse polarity through the loop formed by e-D_1-C-S_2-load-S_4-e. Now since capacitor has some charge, S_1 will turn ON when it is gated. The circuit then follows the normal operation with the capacitor voltage building up with appropriate polarity, each time S_1 and S_2 are switched ON.

Two more cases may arise when the firing pulses are applied to the converter circuit during negative half cycle of supply voltage.

5.3.3 Case III

Suppose the gate pulses are applied to SCRs S_1 through S_4 at instant $t = t_1''$. S_2 and S_3 will start conducting. The charging up of capacitor takes place in the same way as in Case I except that roles of (S_1 and S_2), (S_3 and S_4), (D_1 and D_2) and (D_{L_1} and D_{L_2}) interchange.

In this case the delayed firing of S_4 helps in charging up of capacitor.

5.3.4 Case IV

This may arise when the gate pulses are switched during negative half cycle. Suppose the gate pulses are applied at instant $t = t_1''$ to SCRs S_1 through S_4. S_1 and S_3 will turn ON. The build up of the capacitor charge will be along the lines discussed in Section 5.3.2 for Case II.

The control strategy of Fig. 5.2a is thus considered for developing the firing circuit for the converter circuit of Fig. 4.3.

5.4 FIRING CIRCUIT

The general block diagram of the firing circuit which is suitable for any number of pulses p per half cycle is shown in Fig. 5.3(a). Modifications required in the block diagram for inversion operation is shown in the small diagram of Fig. 5.3(a). For inversion operation, the control signals of Fig. 5.3(b) are assumed. The operation, has been described for five pulses per half cycle for which the circuit diagram is shown in Fig. 5.3(b) and the corresponding waveforms are shown in Fig. 5.3(c). In what follows, the operation of the control circuit is described.

A synchronising signal (A) obtained from 220V AC is transformed into a square wave (B) by a zero cross detector (ZCD). This 50 Hz signal is used as a reference for the phase locked loop (PLL). The PLL in its feedback path has a 'divide by 2(p+1)N' counter, where p is the number of pulses per half cycle of input line frequency. In the present investigation, p is equal to 5. N is kept high to reduce phase errors. The PLL output is fed to a '$\div$ N' counter which is reset at the positive and negative edges of B by means of a signal from a dual edge monostable. This synchronizes the signal output of '$\div$ N counter' [50x2(p+1)] to the line

signal A. The signal B is passed through a ZCD to obtain a ± 12V swing (C),which is integrated and level shifted to obtain a triangular wave (D). The triangular wave is compared with a DC signal (X_c). Compare the comparator output signal (E) with the gating requirements of S_1 during positive half cycle (Fig. 5.1, for five pulses). It can be seen that the initial pulse present in the signal E has to be stretched upto the second pulse and the last pulse occuring in the positive half cycle has to be eliminated. The former has been realized by the following logic :

The inverted signal of comparator output E is fed to the clock of a negative logic (NL) JK Flip Flop (FF) which is kept in the set mode (J = 1, K = 0). The clear signal to this FF comes from the dual edge monostable. The FF gets cleared at the start of the positive and negative synchronising signal. The FF gets set only at the first negative going edge ($\overline{\uparrow}$) of clock,which occurs at the second pulse of the signal E. Thus the output $\overline{Q}$ (F') of FF gives the required signal. This is OR-ed with the comparator output E to get signal G . Still the signal G does not conform to the gating requirements of the SCR S_1. Of course, the gating requirements of S_1 are met by eliminating the last pulse occurring in the positive half cycle which is achieved by the logic described below.

The output of comparator (E) is fed to the clock of a BCD counter, the reset for which comes from the dual edge mono. The

output (H) of the NAND gate remains high till the counter counts six (B = 1, C = 1, D = 0) at which instant H goes low. H remains low till the clear pulse at positive or negative edge of synchronizing signal occurs. Thus we get signal H which remains zero after the sixth pulse of E till the start of the next half cycle. When the signal H is AND-ed with signal G , we get signal I.

The following Exclusive-OR (X-OR) logic realizes the gate signals of Fig. 5.1.

Gate G_2: $K = I \oplus B_1$

Gate G_1: $J = \overline{K}$

Gate G_3: $L = F \oplus B_1$

Gate G_4: $M = \overline{L}$

Fig. 5.2(b) shows the gating requirements for SCRs S_1 through S_4 for the case of regenerative operation of the circuit of Fig. 4.3. The gating signals differ from that of Fig. 5.2(a). The gating signals,as shown in Fig. 5.2(b), help charging up of capacitor.

The modifications required in the control circuit for regenerative operation for the pulse requirements are shown in the small diagram in the dotted rectangle of Fig. 5.3(a). The change in the logic is required only after the signals at the

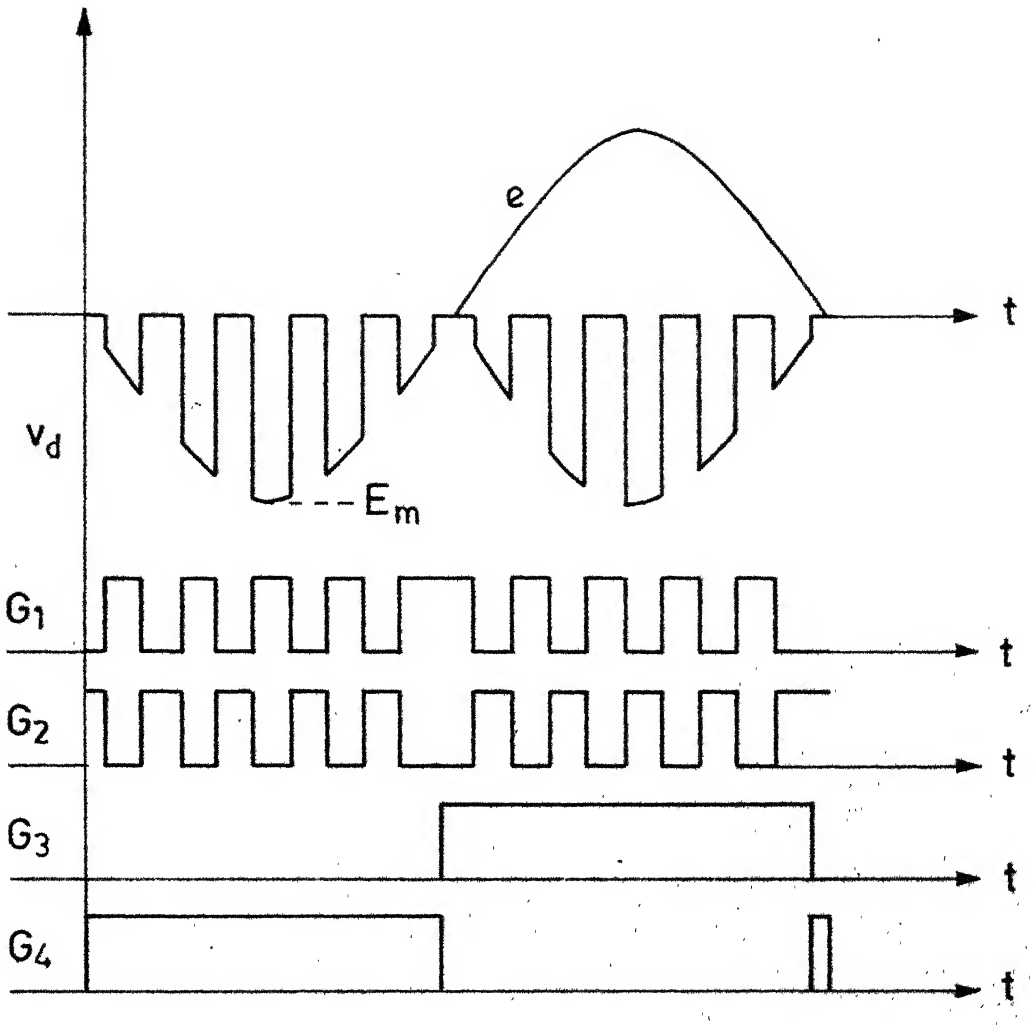


Fig. 5.2 (b) Control signals for SCR S_1 to S_4 for an improved control strategy (Inversion).

output of FF (F and F') and the NAND gate (which is preceded by a BCD counter) output are obtained. The output at the NAND 'H' is inverted and OR-ed with comparator output 'E' to get a signal, 'T'. This signal 'T' is AND-ed with 'F' to get signal 'P'.

The following logic realizes the gate signals of Fig. 5.2(b).

Gate G_1 : $J_1 = P \oplus B_1$

Gate G_2 : $K_1 = \overline{J}_1$

Gate G_4 : $L_1 = \overline{H} \oplus B_1$

Gate G_3 : $M_1 = \overline{L}_1$

Thus we see that the realization for the regenerative operation can be done with a minor change in the logic.

The block diagram of Fig. 5.3(a) is general and can be used for any number of pulses 'p'. The comparator input X_c controls the width of the pulse. When the converter is used in closed-loop operation, the signal X_c represents the feedback voltage signal.

5.5 EXPERIMENTAL SET-UP

The experimental set-up comprises of the following : Firing circuit Fig. (5.3(b)), power circuit (Fig. 4.3) and load. The drive motor is loaded through a separately excited generator which is coupled to it.

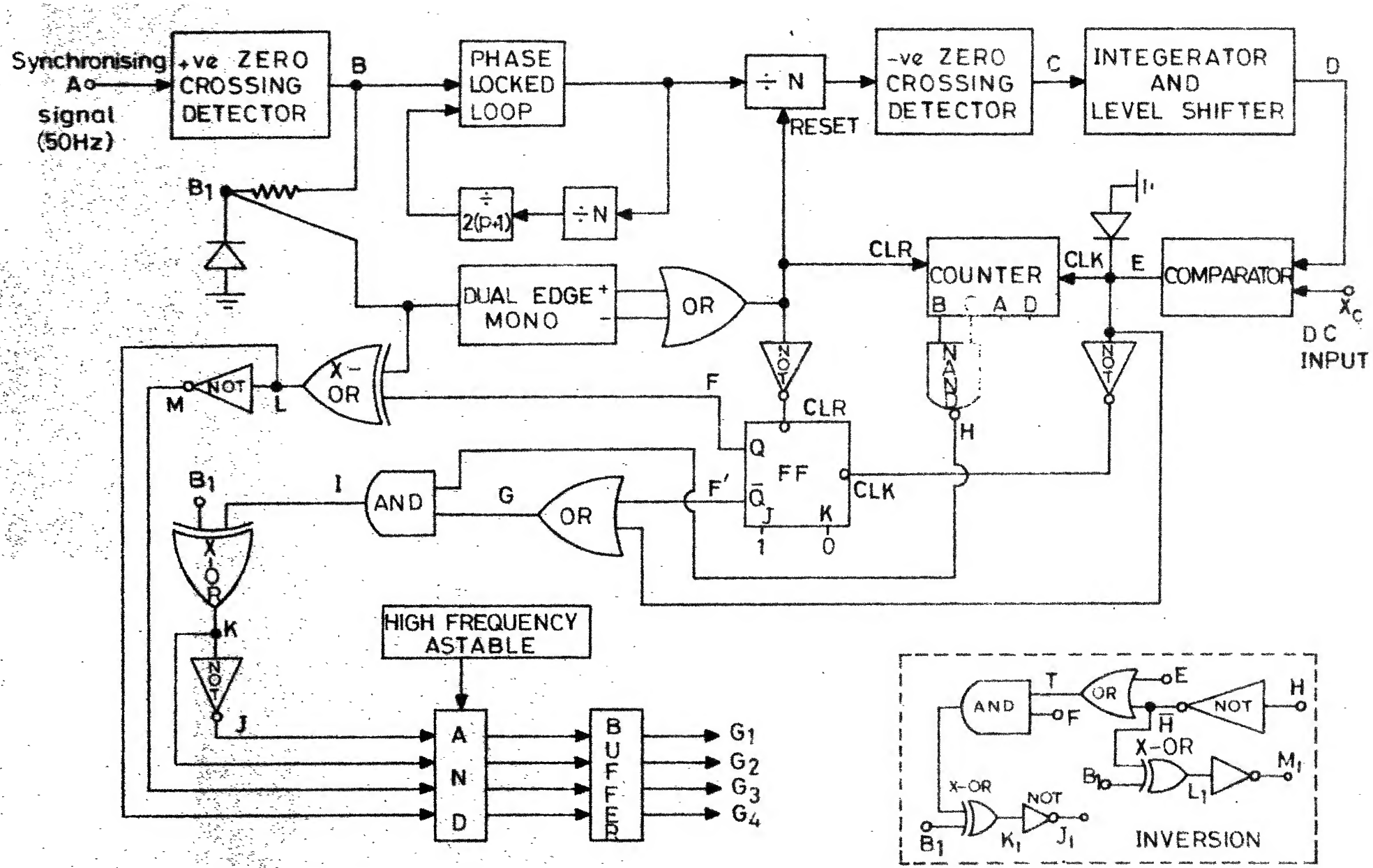


Fig. 5.3 (a) Block diagram of firing circuit to obtain gating signals for SCRs S_1 to S_4 for rectification and inversion.

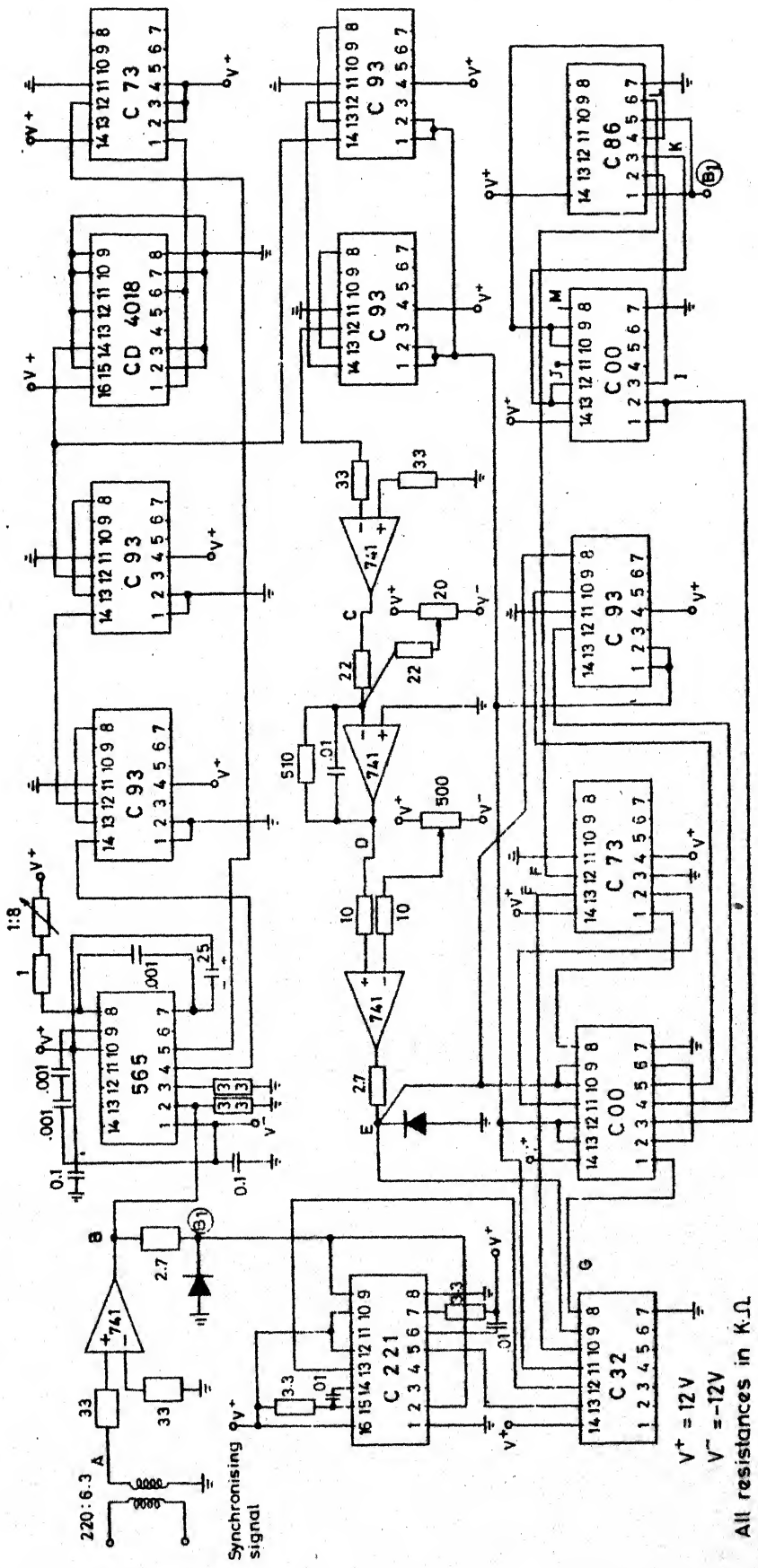


Fig. 5.3(b) Firing circuit for rectification for five pulse per half cycle.

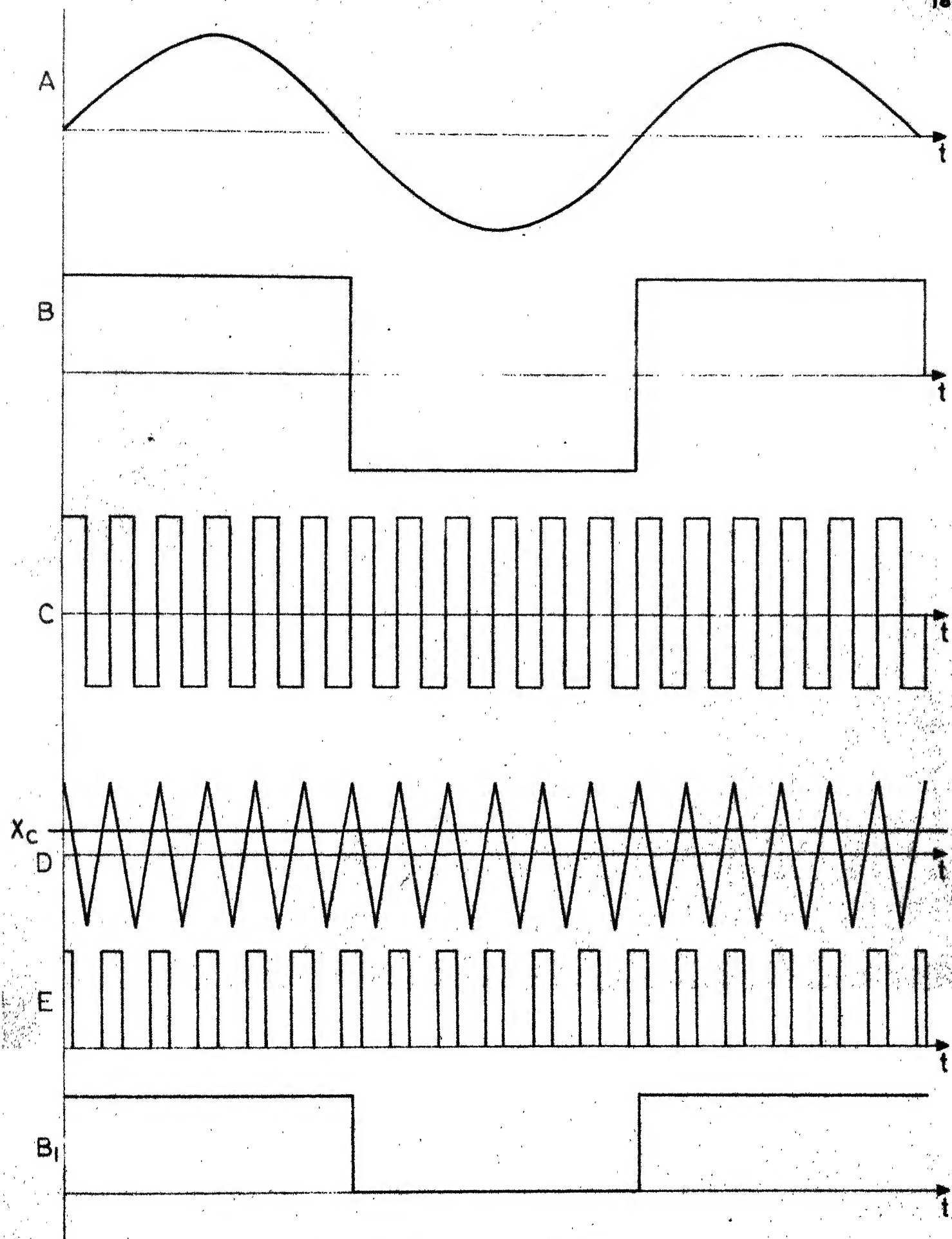


Fig. 5 3 (c) (Contd)

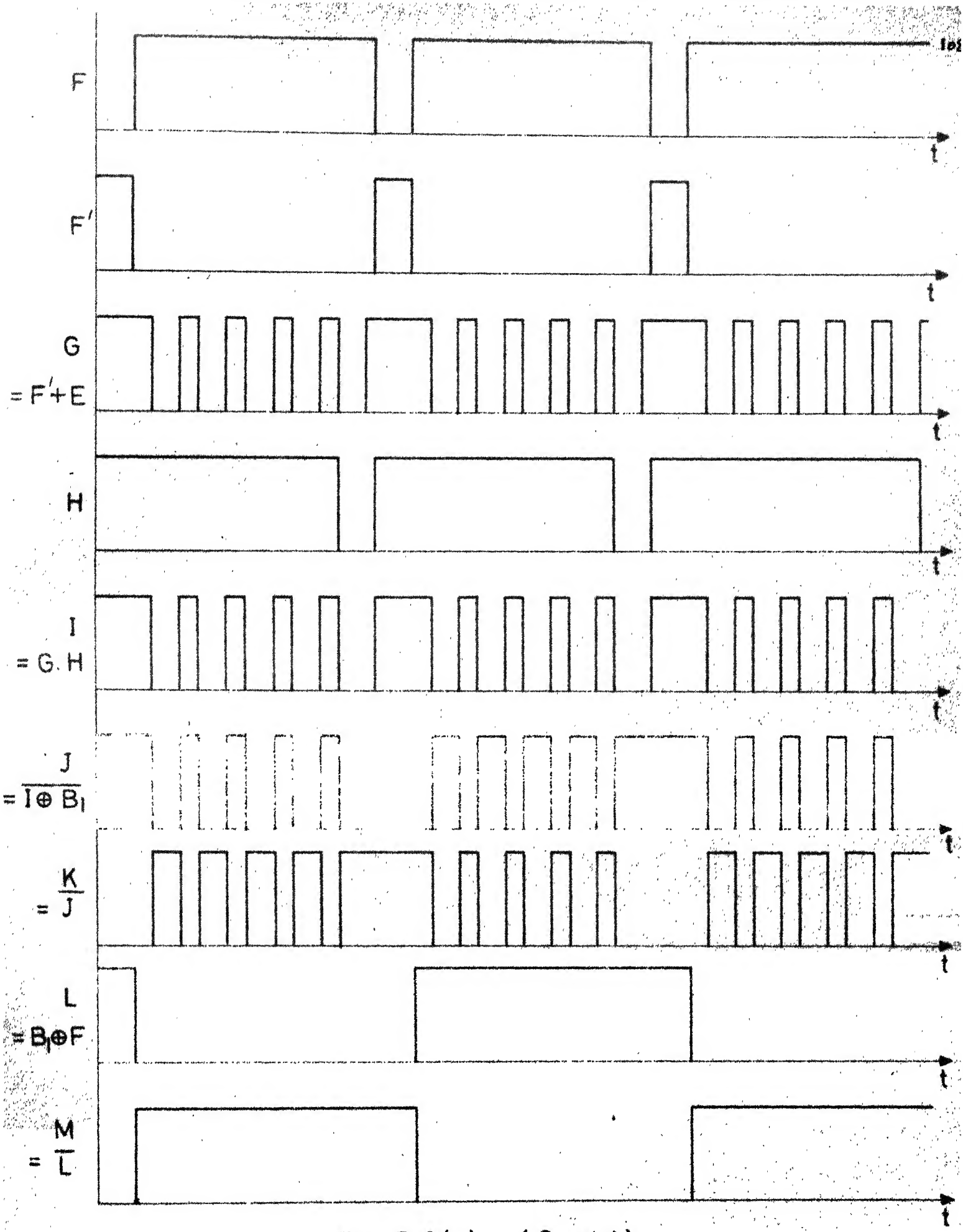


Fig. 5.3(c) (Contd)

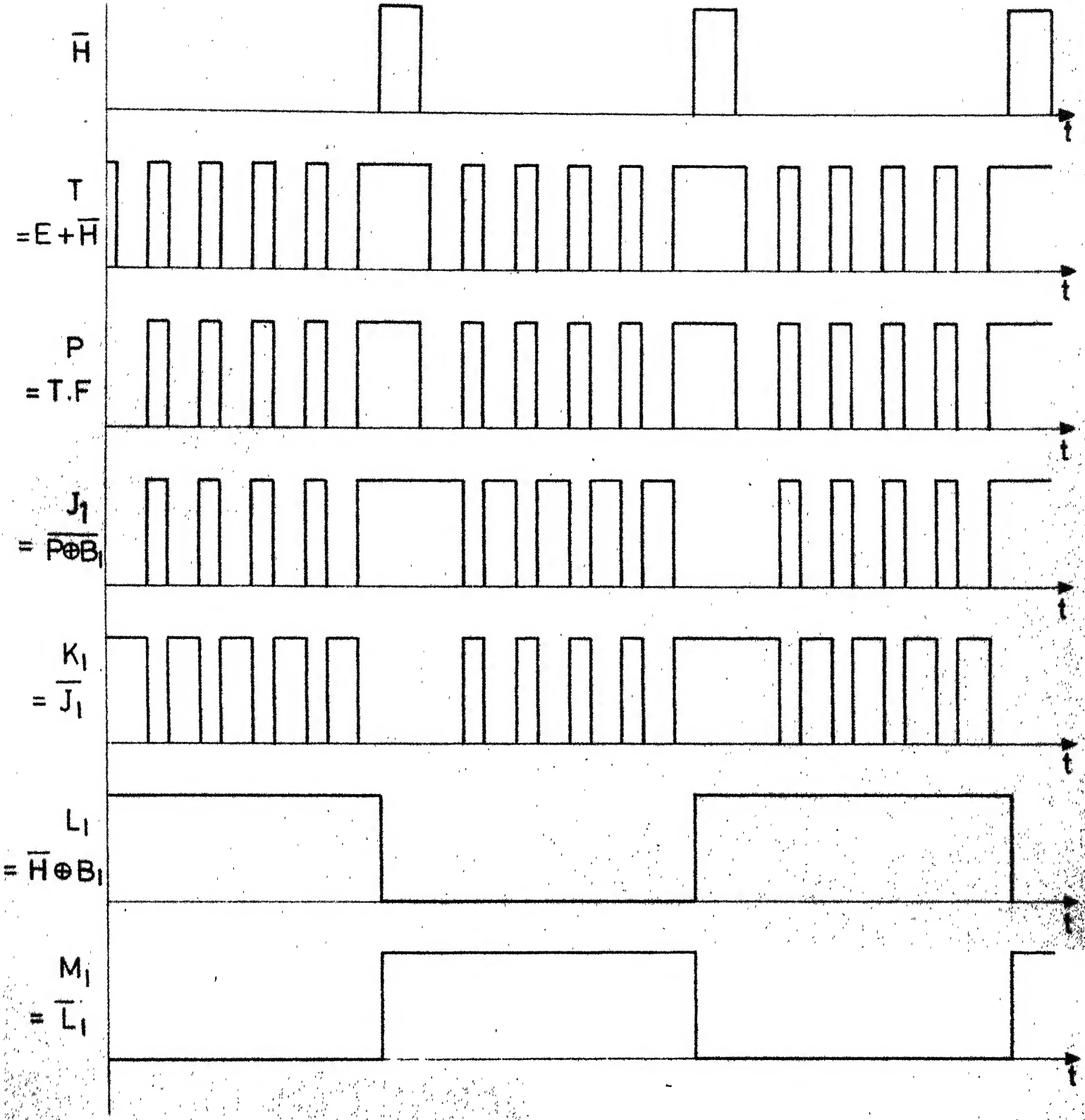


Fig. 5.3(c) Signal at various points indicated.

The pertinent details of the experimental set-up are :

AC input source : 220V, 50 Hz

SCR's S_1 and S_2 : Inverter grade (turn-off time = 25 μsec)
Type No. R36TB6

SCR's S_3 and S_4 : Converter grade
Type No. 26TB12

D_1, D_2 : 12SM15

D_{L_1}, D_{L_2} : 12SM15

Commutating inductor L_1 : 192 μH SWG 15 air cored

Commutating inductor L_2 : 192 μH SWG 15 air cored

Commutating capacitor C : 15 μfd

Source inductance L_s : 0.39 mH SWG 15 air cored

R-L load : R = 21.5 Ohms, L = 80 mH

Motor load : See Appendix I

5.6 EXPERIMENTAL VERIFICATION WITH RL LOAD

Fig. 5.4(a) shows the oscillograms of capacitor voltage and output voltage obtained from the experimental set-up with the modulation index set at 0.4 for R = 21.5 Ohms and L = 80 mH. The predicted results of digital simulation as

described in Sec. 4.6 are given in Fig. 5.4(b) for the same variables. It may be noted that there is a close agreement between the experimental and simulation results.

5.7 EXPERIMENTAL VERIFICATION WITH MOTOR LOAD

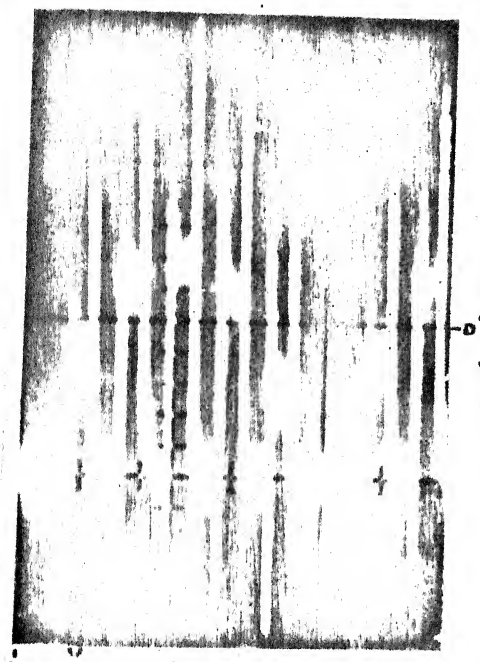
5.7.1 Circuit Behaviour

Separately excited motor, the parameters for which are given in Appendix I, was used as a drive motor. Modulation index was kept at 0.55 with load current maintained at 9.75 amps (by adjusting the load on the coupled generator).

Fig. 5.5(a) shows oscillograms of capacitor voltage V_c and input source current i_s while Fig. 5.5(b) shows the predicted results. The oscillograms for current $i_{D_{L_1}}$ and voltage across SCR S_1 are shown in Fig. 5.6(a) and the corresponding digital simulation results are given in Fig. 5.6(b) respectively. Both experimental and theoretical results agree closely.

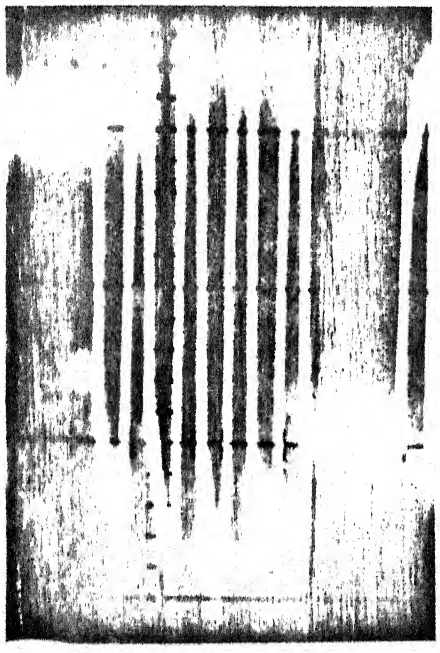
The various modes of operation were also verified experimentally for different pulses in each half cycle of supply voltage. The mode sequence is found to be the same.

A typical set of output voltage and output current oscillograms are shown in Fig. 5.7 for the case of discontinuous conduction at no load (coupled generator is unloaded) with modulation index kept at 0.55.



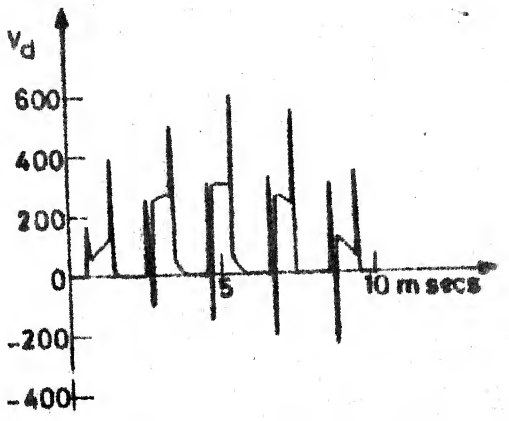
x axis
1cm = 5m secs
y axis
1cm = 200 volts

(1) Output voltage, V_d

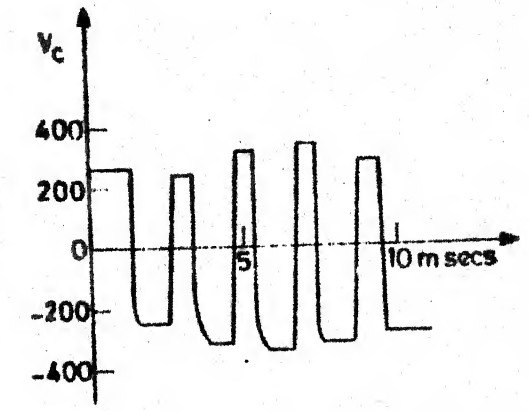


(2) Capacitor voltage, V_c

Fig.5.4(a) Experimental waveforms for R-L load

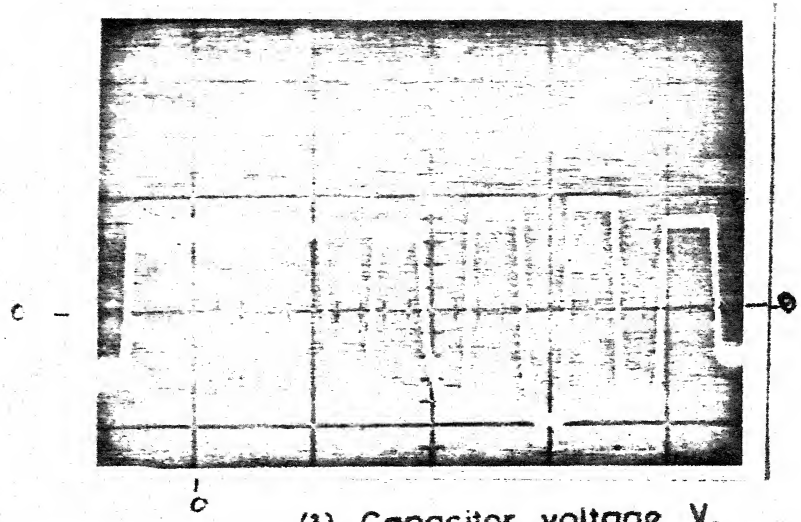


(1) Output voltage V_d

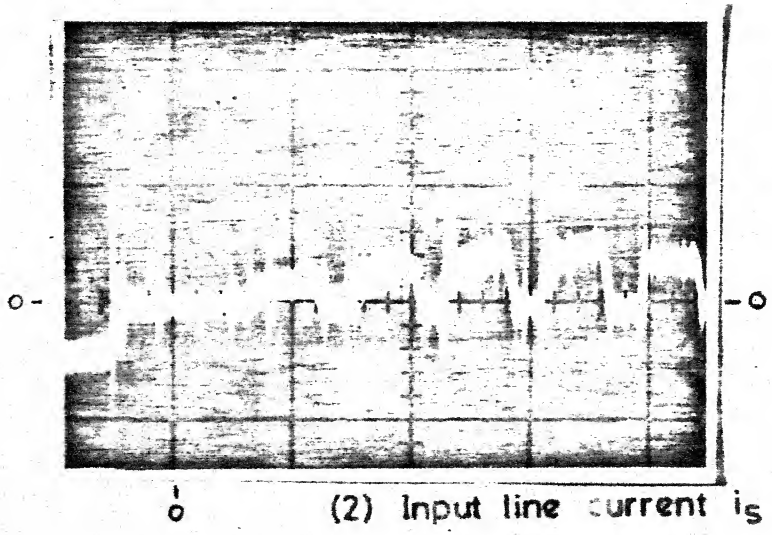


(2) Capacitor voltage V_c

Fig.5.4(b) Theoretical waveforms for R-L load.

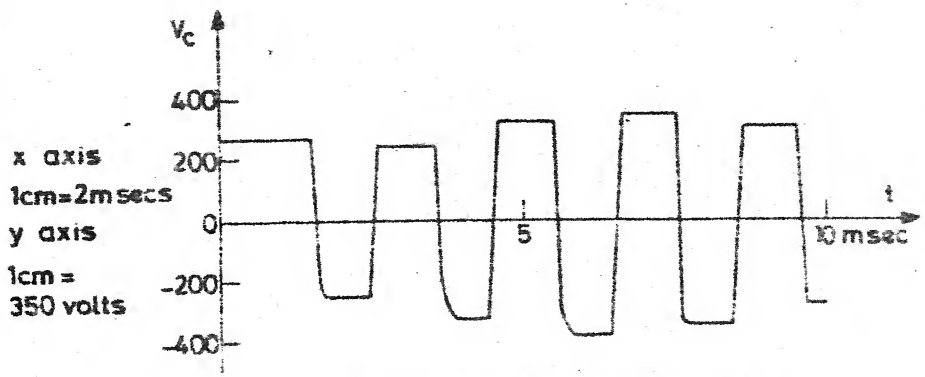


(1) Capacitor voltage V_c

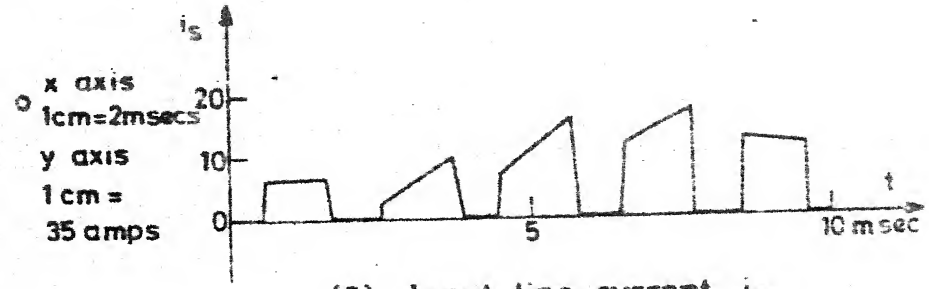


(2) Input line current i_s

Fig.5.5(a) Experimental waveforms for motor load.



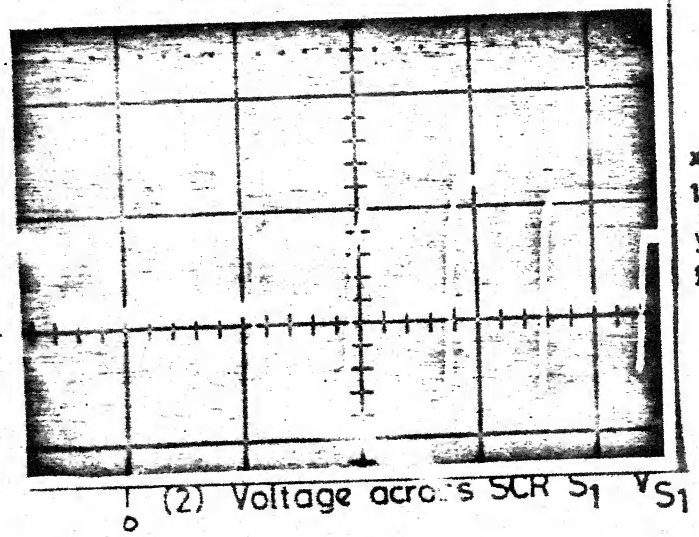
(1) Capacitor voltage V_c



(2) Input line current i_s

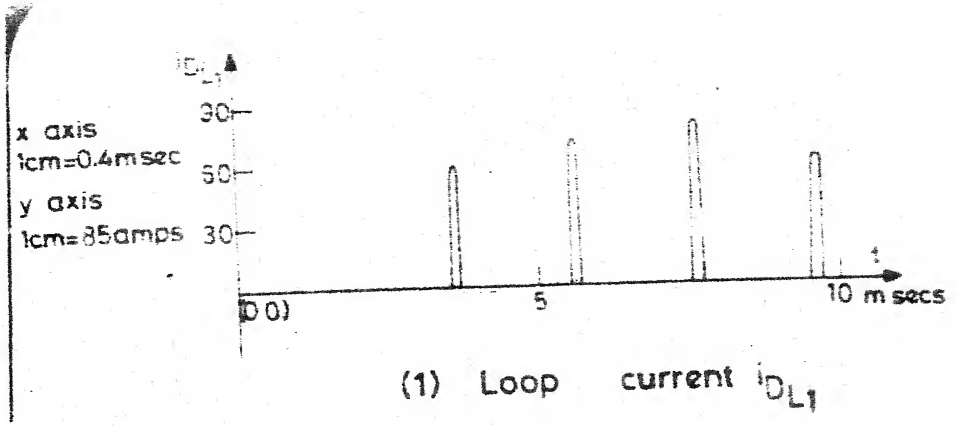
Fig.5.5(b) Theoretical waveforms for motor load.

(1) Loop current i_{D_1}.

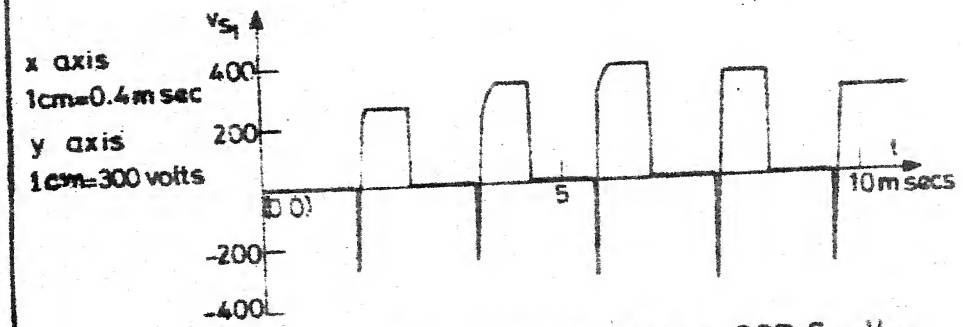


(2) Voltage across SCR S_1 V_{S_1}

Fig.5.6(a) Experimental waveforms for motor load.

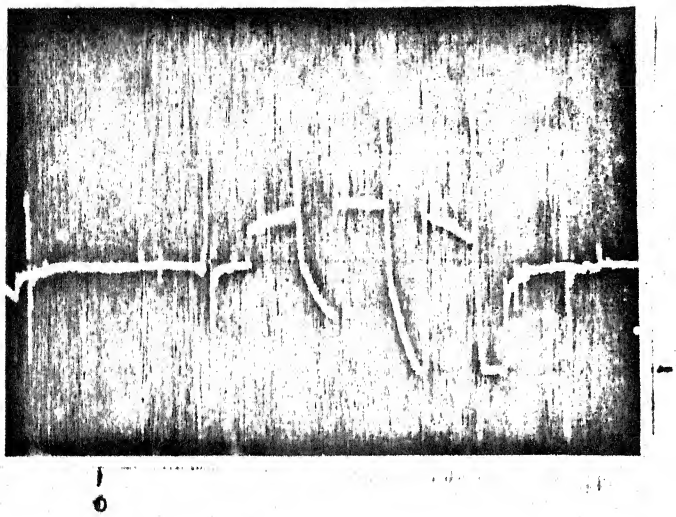


(1) Loop current i_{D_1}



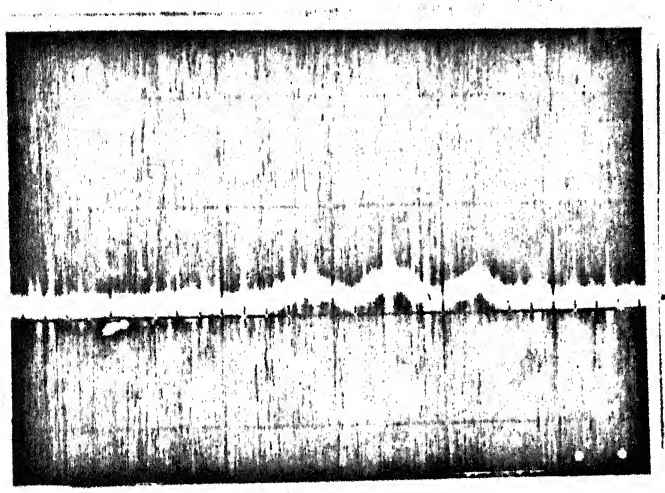
(2) Voltage across SCR S_1 V_{S_1}

Fig.5.6(b) Computed waveforms for motor load.



x axis
1 div = 2 m sec.
y axis
1 div = 200 volts

(a) Output voltage v_d



x axis
1 div = 2 m sec
y axis
1 div = 10 amps

(b) Output current i_d

Fig. 5.7 Typical output voltage and current waveforms for motor load (at no load). (Discontinuous)

5.7.2 Speed-torque Characteristics

For a fixed value of modulation index and pulse number (= 5), the armature current i_d was varied and the motor speed 'N' was noted corresponding to each armature current.

The back emf E was calculated using the equation

$$E = \frac{Kb \cdot 2\pi N}{60}$$

The speed and torque are normalized by the following base values.

Base value for voltage $= \frac{2\sqrt{2}\ 220}{\pi} = 197$ volts

Base value for current $= \frac{197}{2.192} = 90$ amps.

Fig. 5.8 shows the normalized speed v/s torque characteristic. Also shown in Fig. 5.8 is the simulation results taking commutation transients into account. There appears to be a close agreement between predicted and measured results.

5.7.3 Power Factor Variation

Power factor is defined as :

$$\text{Power factor} = \frac{V_d \times I_d}{V_{rms} \times I_{rms}}$$

where V_d = average output voltage of converter

I_d = average output current of converter

V_{rms} = line rms voltage

I_{rms} = line rms current.

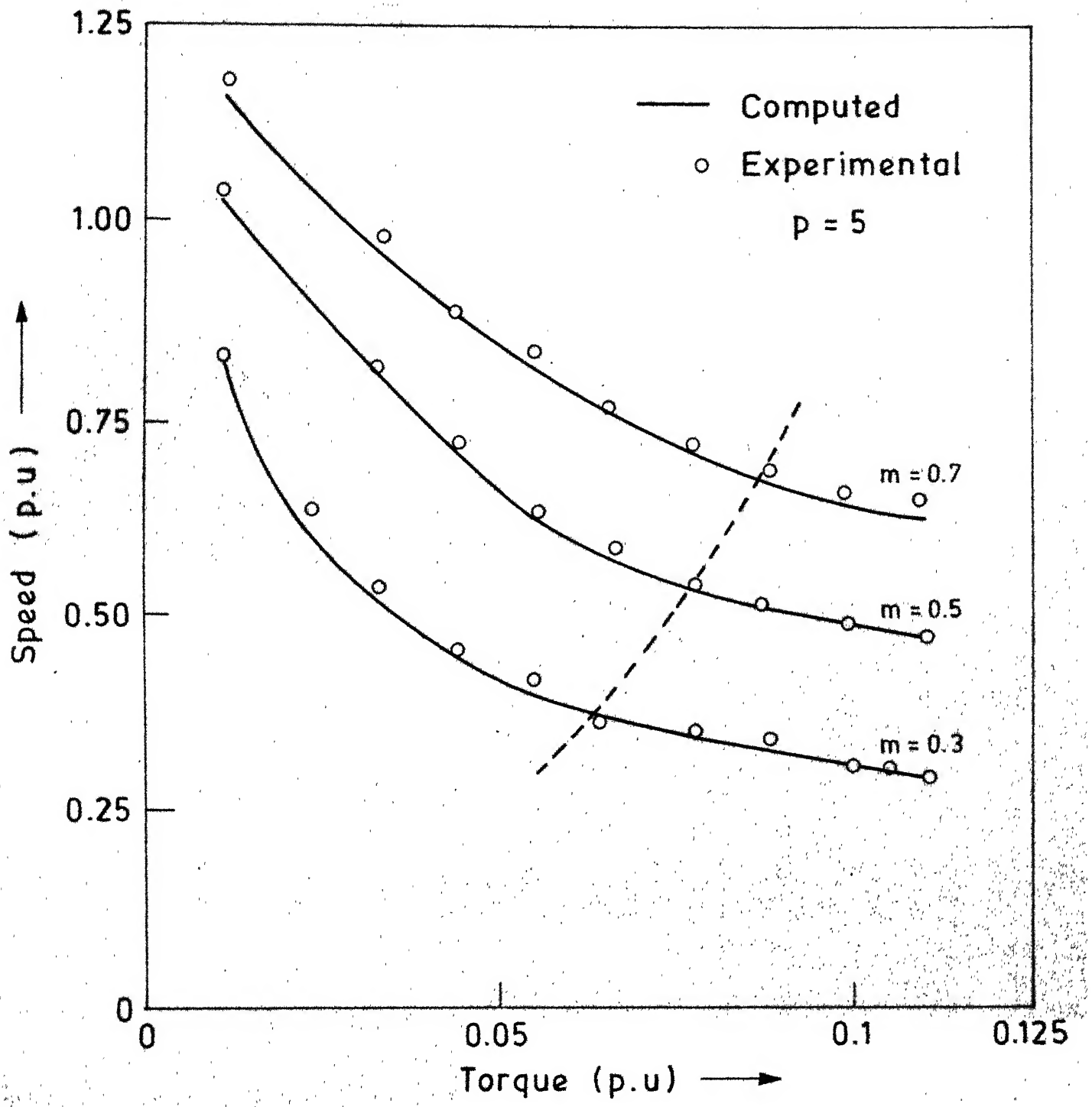


Fig. 5.8 Experimental verification of speed-torque characteristics.

The power factor for each value of load current is calculated by measuring I_d, V_{rms} (constant 220V, 50 Hz) I_{rms} and V_d.

Fig. 5.9 shows a plot of experimental and predicted power factor variation with load current for different values of modulation index.

Since the input current is non-sinusoidal an accurate rms meter is required to measure I_{rms}. Due to non-availability of true rms meter in the laboratory, a moving iron instrument was used to measure I_{rms}. The experimental and predicted results agree satisfactorily. The apparent discrepancy may be attributed, to the error involved while measuring 'I_{rms}',

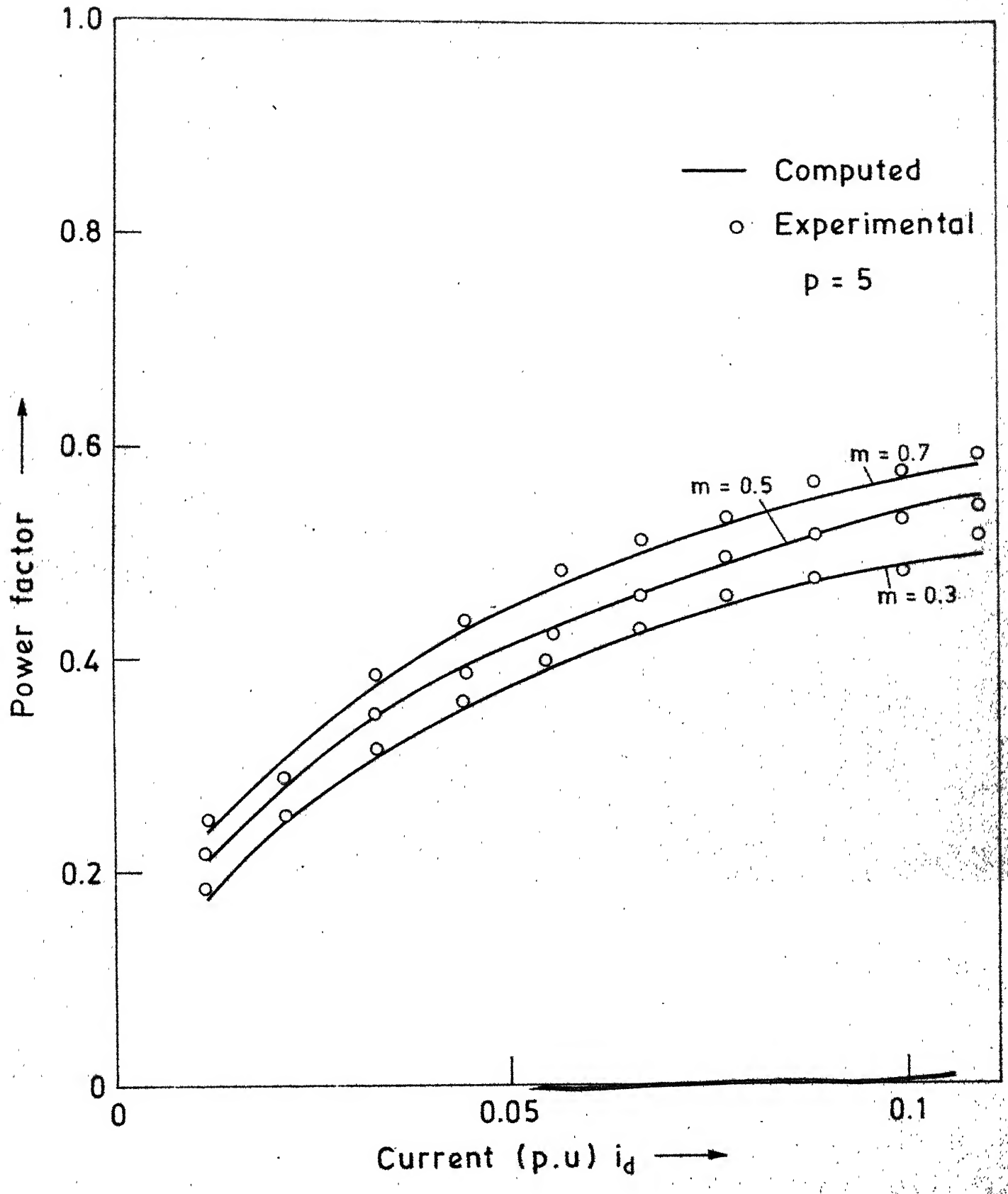


Fig. 5.9 Experimental verification for power factor.

CHAPTER VI

CONCLUSIONS

6.1 CONCLUSION

A simple and versatile pulse-width controlled ac-dc converter has been studied in this thesis. It works satisfactorily with both passive load (RL) and active loads (separately excited dc motor).

The equal pulse-width modulation scheme provides a wide variation of output voltage. The output voltage varies linearly with control variable 'modulation index' for pulse greater than two in each half cycle of supply voltage. Equal pulse-width modulation with five pulse per half cycle seems to be optimum from the consideration of voltage variation range, linearity of output voltage and suppression of lower input harmonic contents.

The study of input and output performances of a pulse-width controlled ac-dc converter fed DC motor shows that the pulse-width controlled converter has several advantages over phase delay controlled converter from the following considerations :

1. The input displacement factor is close to unity over a wide range of output current. As a result of this power factor is improved considerably.

2. The harmonics in the input line current shift from lower order components to higher order components. This makes the filtering problem relatively easy since small sized filter components are required to filter them.

3. Because of several switchings in each half cycle, the output current is continuous over a wide range of speed and torque. This may improve the transient response of the drive system. Also it may have higher efficiency, lesser cost, smaller size and weight since small sized filter inductor is generally required.

The detailed digital simulation of the converter with RL and motor load shows that the modes of operation and their sequences remain the same for both types of load for continuous output current.

This converter with a particular triggering strategy does not require precharging of commutating capacitor while starting the converter initially.

Investigation of speed-torque characteristics with and without commutation effects show that they depart considerably at lower values of modulation index. However, by using SCRs of low turn-off time and also by a judicious choice of commutation circuit parameters, the commutation transients can be minimized. As a result, the speed-torque characteristics with and without commutation effects approach each other.

It has been observed that the turn-off time offerred to SCRs S_1 is lower that of SCR S_2. This is due to the overcharging of commutating capacitor whenever S_2 conducts. The turn-off generally decreases with an increase in the load current. In this equal pulse-width scheme with five pulses per half cycle and modulation index of 0.5 there is a reduction of 11.5 percent in the turn-off time offered to S_1 from the ideal designed value of 84.25 μsecs,at rated load current.

6.2 SCOPE FOR FURTHER WORK

The analysis of the converter-motor system using the method described in Chapter 4 may be carried out for the discontinuous current conduction case.

Since the spectrum of frequencies shift from lower to the higher, line side filters are to be used to suppress the higher order harmonics which further minimizes reactive power requirement from the ac supply line. It may be very interesting to look into the closed loop motor speed control with pulse-width modulation. The disadvantage of discontinuous current conduction which arises in phase delay control may be overcome. It is expected that the transient response with PWM will be improved.

In this thesis studies are limited to rectifier operation with the drive system operating in motoring mode. Since the converter operates equally well in regenerative mode,

Studies may be undertaken to investigate this with both continuous and discontinuous conduction.

Lastly, the four quadrant operation with a motor load may be investigated with two pulse-width ac-dc converters. It may overcome all the disadvantages of a phase-controlled dual converter. However, it may not be economical but the improvements in the line side and motor side performances may justify forced commutated dual converter.

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APPENDIX I

LUMPED CIRCUIT IMPEDANCE REPRESENTATION FOR DC MACHINES

A lumped constant equivalent circuit as suggested by Ewing [18] is shown in Fig. A-1 below.

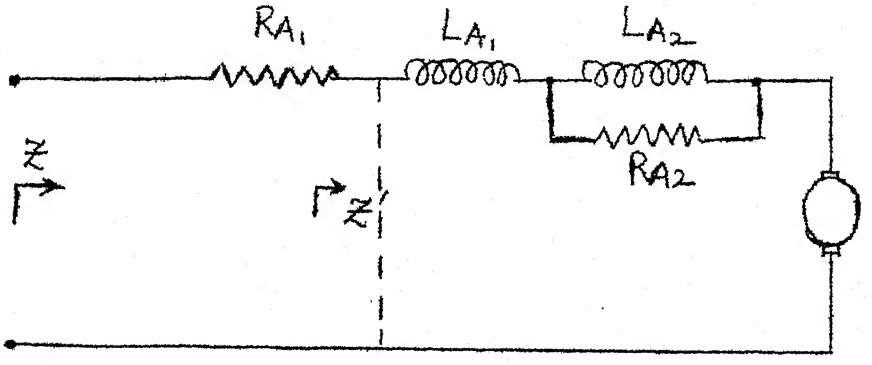

Fig. A-1

where

R_{A_1} = armature circuit resistance

R_{A_2} = fictitious shunting resistance

$L_{A_1}+L_{A_2}$ = total armature circuit inductance.

The above equivalent lumped circuit constants can be derived from locked armature impedance measurement at a series of different frequencies. Fig. A-2 shows the test circuit which can be utilized for determining the constants, noting down the frequency, ac current, ac voltage and power fed.

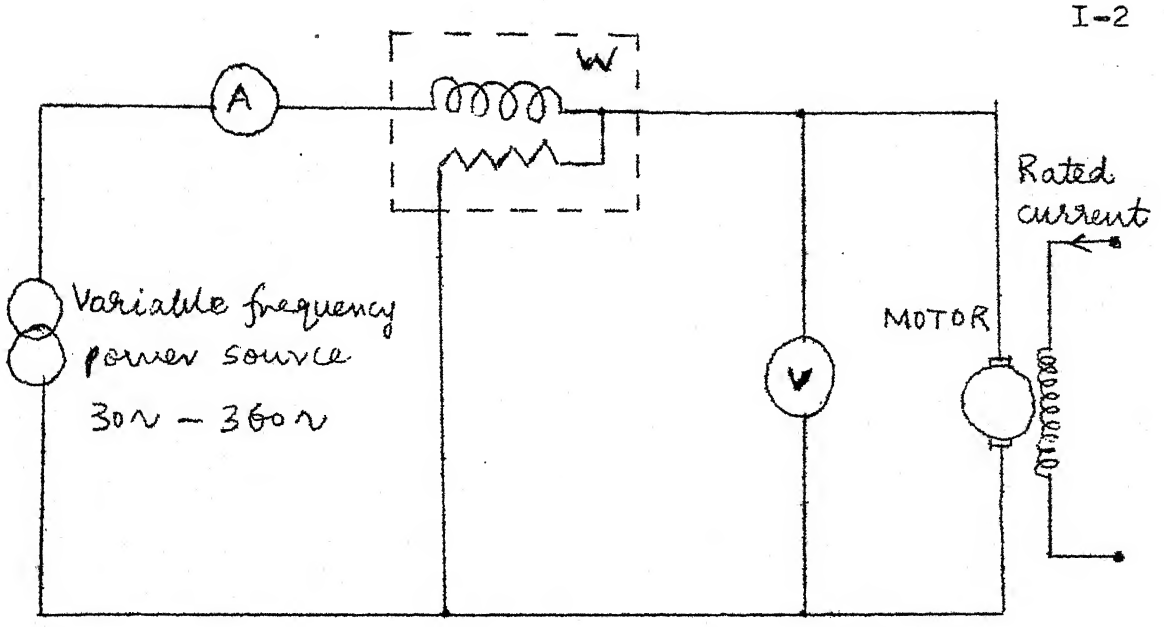

Fig. A-2

The constants were found out for a 3 hp, 1450 r/min, 220 volts motor having an armature resistance R_{A_1} = 2.192 ohms.

The calculated lumped circuit constants at rated field current are found to be,

R_{A_2} = 4.6 ohms.

L_{A_1} = 17.5 mH .

L_{A_2} = 5.3 mH .

Since the output harmonics of an equal pulse-width controlled converter are very less, the eddy current model was found only for frequency corresponding to the speed of the motor.

The motor back emf constant (K_b) was found to be $K_b = 1.378V/rad/sec$. The motor is run as a generator and an emf vs speed curve is plotted. From this curve the back emf constant ($K_b = \frac{E_b}{w}$) is calculated.

APPENDIX-II-A.

```
C
C  THE FOLLOWING IS THE LISTING OF THE SIMULATION PROGRAM WHICH
C  FINDS THE VARIOUS MODES OF OPERATION OF A FORCED COMMUTATED
C  CONVERTER FEEDING A D.C.MOTOR.     TORQUE IS INITIALLY ASSUMED
C  AND THE SPEED CORRESPONDING TO IT FOR A PARTICULAR VALUE OF
C  MODULATION INDEX AND PULSE NO.FOUND OUT.      A PARTICULAR MODE
C  IS ASSUMED AND THE OTHER MODES ARE THEN FOUND OUT ONLY OVER
C  A HALF CYCLE(AS THE OPERATION IS SAME OVER THE NEXT HALF CYCLE
C  ).     ITERATIONS ARE CARRIED ON TILL THE STEADY STATE IS
C  REACHED.
C  STEP WIDTH DURING COMMUTATION IS CHANGED(REDUCED) TO FOLLOW
C  IT MORE CLOSELY.  WHEN DIODES D(1),D(2) CONDUCT THE MOTOR
C  CURRENT IS ASSUMED TO BE CONSTANT,MOTOR SPEED IS ASSUMED TO BE
C  CONSTANT OVER THE HALF CYCLE,INDUCTANCE AND RESISTANCE ARE
C  ALSO ASSUMED TO BE CONSTANT.  THE EDDY CURRENT MODEL OF THE
C  MOTOR WAS UTILIZED TO FIND ITS RESISTANCE AND INDUCTANCE.
C        THE NUMERICAL METHOD USED FOR SOLVING THE DIFFERENTIAL
C   EQUATIONS IS   "FULERS".
C
C           DEFINITION OF VARIABLES
C
C  SS=THY.VARIABLE,DD=DIODE VARIABLE,DL=LOOP DIODE VARIABLE
C    SS,DD,DL ARE LOGIC VARIABLES
C  ISS=THY.CURRENT,IDD=DIODE CURRENT,IDL=LOOP DIODE CURRENT
C  VSS=THY.VOLTAGE,VDD=DIODE VOLTAGE,VDL=LOOP DIODE VOLTAGE
C  VD=DIODE DROP,VS=THYRISTOR DROP
C  Z1,Z2,Z3,Z4,Z5 ARE THE FIVE STATE VARIABLES
C  WHERE Z1=LOOP1 CURRENT,Z2=LOOP2 CURRENT,Z3=OUTPUT CURRENT,
C  Z4=CAP.VOLTAGE,Z5=INPUT LINE CURRENT
C  X=PRESENT VALUE OF LOOP1 CURRENT,XI=LAST VALUE OF IT,
C  L1=LOOP1 COMMUTATING INDUCTANCE
C  ZZ=PRESENT VALUE OF LOOP2 CURRENT,ZZI=LAST VALUE OF IT,
C  L2=LOOP2 COMMUTATING INDUCTANCE
C  Y=PRESENT VALUE OF CAP. VOLTAGE,YI=LAST VALUE OF IT,
C  C=COMMUTATING CAPACITANCE
C  WW=PRESENT VALUE OF INPUT CURRENT,WI=LAST VALUE OF IT,
C  V=PRESENT VALUE OF OUTPUT CURRENT,VI=LAST VALUE OF IT,
C  E=THE MOTOR BACK E.M.F.,EM=INPUT LINE MAX. VOLTAGE
C  T=TIME,W=ANGULAR FREQUENCY,RA1=ARMATURE CIRCUIT RESISTANCE
C  RA2=FICTITIOUS SHUNTING RESISTANCE,(LA1+LA2)=TOTAL ARMATURE
C  CIRCUIT INDUCTANCE,RA=EQUIVALENT RESISTANCE OF ARM.CIRCUIT
C  LA=EQUIVALENT INDUCTANCE OF ARM.CIRCUIT,LS=INPUT SOURCE IND.
C  VC=CAPACITOR VOLTAGE,B=FIRING PULSE LOGIC VARIABLE,
C  H=STEP OF INTEGERATION,OUT=OUTPUT VOLTAGE,
C  FL1,FL2,FL3,FL4,FL5,FL6,FL7,FL8,FL9,FL10,FL11,FL12 ARE THE
C  FLAG VARIABLES,EACH CORRESPONDING TO A PARTICULAR MODE.IT IS
C  USED FOR PRINTING PARTICULAR MODE,
C  AM=MODULATION INDEX,N=PULSE NO.,
C  VDC=AVG.VOLTAGE,EMM=INITIAL VALUE OF CAP.VOLTAGE,
C  ZZ1,ZZ2 ARE THE VALUES OF STATE VARIABLES Z1,Z2 RESP. AT THE
C  BEGINNING OF THE HALF CYCLE.
C  PI=CONSTANT,TOR=INITIAL TORQUE AT BEGINNING OF HALF CYCLE,
C  E1=ALLOWABLE ERROR IN OUT.CUR.,E2=ALLOWABLE EERROR IN CAP.VOL.
C  J=SHOWS THE NO.OF STEPS FOR WHICH CALCULATIONS DONE AT ANY
C  INSTANT OF TIME.
C  IINIT,VCINIT,Z1INIT,Z2INIT,Z5INIT ARE THE VALUES OF OUTPUT
C  CURRENT,CAP.VOLTAGE,LOOP1 CURRENT,LOOP2 CURRENT AND INPUT
C  CURRENT RESPECTIVELY AT TIME=0.0
C  FREQ=LINE FREQUENCY,KB=BACK EMF CONSTANT,CUR=LOAD CURRENT
C  MM=NO. OF STEPS OF INTEGERATION,
C  IFINAL,VCFINA,Z1FINA,Z2FINA,Z5FINA ARE THE VALUES OF OUTPUT
C  CURRENT,CAP.VOLTAGE,LOOP1 CURRENT,LOOP2 CURRENT AND INPUT
C  CURRENT RESPECTIVELY AT THE END OF HALF CYCLE
C  IAVG=CALCULATED CURRENT(AVG)OVER HALF CYCLE
C  TD=TORQUE CALCULATED FROM IT
C  SP=SPEED FOR THE ABOVE TORQUE
```

```
      REAL ALFA(50),BETA(50),IDC,IINIT,IDL,L1,L2,LA,LS,IDD,ISS,IFINAL
      REAL KB,IAVG,LA1,LA2
      DIMENSION TT(1000)
      COMMON/LOGIC/SS(5,1000),DD(5,1000),DL(5,1000),J
      COMMON/CUR/ISS(5),IDD(5),IDL(5)
      COMMON/VOL/VSS(5),VDD(5),VDL(5)
      COMMON/DROP/VD,VS
      COMMON/STATE/Z1(1000),Z2(1000),Z3(1000),Z5(1000)
      COMMON/STATE1/Z4(1000)
      COMMON/LOOP1/X,XI,L1
      COMMON/CAP/Y,YI,C
      COMMON/OCUR/V,VI
      COMMON/ICUR/WW,WI
      COMMON/LOOP2/ZZ,ZZI,L2
      COMMON/TIME/E,EM,T,W
      COMMON/PAR/RA,LA,LS
      COMMON/CAPVO/VC
      COMMON/FIRING/B(5)
      COMMON/STEP/H
      COMMON/VOUT/OUT(1000)
      COMMON/FLAG/FL1,FL2,FL3,FL4,FL5,FL6,FL7,FL8,FL9,FL10,FL11,FL12
      READ*,ZZ1,ZZ2,FREQ,EM,RA1,RA2,L1,VS,VD,C,L2,LA1,LA2,LS,CUR,KB
      Z1(1)=ZZ1;Z2(1)=ZZ2;FL10=1.
C     ------------------------------------------------------------------
CCC   | PRINTING OF VARIOUS DESCRIPTIONS AND HEADING DONE               |
C     ------------------------------------------------------------------

      PRINT 1
      PRINT 1
1     FORMAT(1X,130('*'))
      PRINT 9
9     FORMAT(/1X,'**  "AS AN INITIAL CONDITION S(2),S(4) AND D(2) ARE
     1 ASSUMED TO BE CONDUCTING"  **'/)
      PRINT 1
      PI=3.1416;FLAG=0.0
C     ------------------------------------------------------------------
CCCC  | CALCULATION OF BACK E.M.F.USING TORQUE(ASSUMED),CALCULATION OF  |
CCCCC | MOTOR RESISTANCE AND INDUCTANCE USING EDDY CURRENT MODEL.ALSO   |
CCCCC | INITIALIZATION OF CURRENTS IN DEVICES AND STATE VARIABLES DONE  |
C     ------------------------------------------------------------------

      W=2.*PI*FREQ
      TOR=CUR*KB
      N=5
      M=5
      AM=M/10.
      CALL ALBE(ALFA,BETA,AM,N)
      CALL RATIO(ALFA,BETA,N,R)
      VDC=2.*EM*R/PI
      E=VDC-CUR*RA
      WWE=E/KB
      SPEDS=WWE*60./(2.*PI)
      FRR=SPEDS*4./120.
      WFRR=2.*PI*FRR
      G=RA2**2+(WFRR*LA2)**2
      RA=RA1+(((WFRR*LA2)**2)*RA2)/G
      LA=LA1+(LA2*(RA2**2))/G
      EMM=EM+CUR*SQRT(LS/C)
      ISS(2)=CUR;ISS(4)=CUR;IDD(2)=CUR
      Z3(1)=CUR;Z4(1)=-EMM;Z5(1)=0.0
      PRINT 121,Z1(1),Z2(1),Z3(1),Z4(1),Z5(1)
```

```
121     FORMAT(1X,'THE INITIAL VALUES OF THE STATE VARIABLES ARE:',1X,'Z
        11=',F4.2,',','Z2=',F4.2,',','Z3=',F5.2,',','Z4=',F7.2,',','Z5='
        1,F4.2)
        PRINT 1
        E1=CUR/100.
        E2=EMM/100.

C       ------------------------------------------------------------------
CCC     | INITIALIZATION OF ALL STATE VARIABLES DONE                      |
        ------------------------------------------------------------------

245     IINIT=CUR
120     VCINIT=-EMM
150     Z1INIT=0.0
201     Z2INIT=0.0
203     Z5INIT=0.0
205     VI=IINIT
        YI=VCINIT
        WI=Z5INIT
        XI=Z1INIT
        ZZI=Z2INIT
        T=0.0;J=2;AI=0.0

C       ------------------------------------------------------------------
CCCC    | THE LOGIC VARIABLE VALUES OF THY.,DIODE,LOOP DIODE AND GATE    |
        | FIRING ARE FOUND                                               |
        ------------------------------------------------------------------

80      CALL MODE(T,B,AM,FREQ,N)
        CALL DIODE(IDL,DL,VDL,J)
        CALL DIODE(IDD,DD,VDD,J)
        CALL THYRIS

C       ------------------------------------------------------------------
CCC     | STEP LENGTH CHOSEN ACCORDINGLY                                 |
        ------------------------------------------------------------------

        IF(DL(1,J).EQ.1.)GO TO 16
        IF(DL(2,J).EQ.1.)GO TO 16
        H=0.00002
        GO TO 14
16      H=0.000006

C       ------------------------------------------------------------------
CCCCC   | ALL THE VALUES OF STATE VARIABLES,CURRENTS IN THY. AND DIODES   |
        | ,VOLTAGES IN THY.AND DIODES ARE FOUND OUT AT EACH INSTANT OF    |
        | TIME,LOOKING INTO WHETHER THE OUTPUT CURRENT HAS GONE DOWN TO   |
        | ZERO(i.e.DISCONTINOUS CONDUCTION)OR NOT                         |
        ------------------------------------------------------------------

14      CALL LOOP21
        Z1(J)=X
        CALL LOOP12
        Z2(J)=ZZ
        CALL OUTCUR
        Z3(J)=V
        AI=AI+V
        CALL CAPVOL
        Z4(J)=Y
        IF(Z3(J).GT.0.0)GO TO 30
        CALL DISVOL
        DO 40 I=1,2
        IDL(I)=0.0;IDD(I)=0.0
40      CONTINUE
        DO 50 I=1,4
        ISS(I)=0.0
```

```
50      CONTINUE
        GO TO 70
30      IF(DD(1,J).NE.1.)GO TO 10
        IF(DD(2,J).NE.1.)GO TO 10
        CALL INPCUR
        Z5(J)=WW
        CALL BOTH
10      CALL OUTVOL
        CALL VOLTAG
        IF(DD(1,J).NE.1.)GO TO 60
        IF(DD(2,J).NE.1.)GO TO 60
        GO TO 70
60      IF(SS(1,J).EQ.1.)GO TO 66
        IF(SS(2,J).EQ.1.)GO TO 66
        GO TO 68
66      IF(DD(1,J).EQ.1.)GO TO 69
        GO TO 68
69      Z5(J)=Z3(J)
        WW=Z3(J)
68      CALL CURREN
70      XI=X;YI=Y;ZZI=ZZ;VI=V;WI=WW
        T=T+H
        TT(J)=T
        J=J+1
        IF(T.LT.0.01)GO TO 80
        MM=J-1
        VCFINA=Y;IFINAL=V;Z1FINA=X;Z2FINA=ZZ;Z5FINA=WW
        IF(FLAG.EQ.0.0)GO TO 71

C     ------------------------------------------------------------------
CCC   | THE CONVERGENCE OF FINAL TO INITIAL OUTPUT CURRENT SEEN AND     |
CCC   | THE INITAL VALUE CORRECTED ACCORDINGLY                          |
C     ------------------------------------------------------------------

        IF(ABS(IINIT-IFINAL).GT.(2.*E1))GO TO 85
        GO TO 72
71      IF(ABS(IINIT-IFINAL).GT.E1)GO TO 85
72      IAVG=AI/MM
        TD=IAVG*KB

C     ------------------------------------------------------------------
CCC   | THE CONVERGENCE OF CALCULATED TORQUE TO ASSUMED TORQUE SEEN     |
CCC   | AND THE BACK EMF CORRECTED ACCORDINGLY TO CORRESPOND TO TORQUE  |
C     ------------------------------------------------------------------

        IF(ABS(TD-TOR).LT.0.5)GO TO 220
        IF(TD.LT.TOR)GO TO 250
        IF(ABS(TD-TOR).GT.(5.*0.1))GO TO 240
        E=E+0.1
        GO TO 249
240     E=E+1.
        GO TO 249
250     DO 235 KKK=1,MM
        IF(Z3(KKK).NE.0.0)GO TO 235
        IF(AM.LE.0.6)GO TO 237
        GO TO 239
235     CONTINUE
239     E=E-0.25
        GO TO 249
237     E=E-1.
249     IF(E.GT.0.0)GO TO 245
        PRINT 199
199     FORMAT(5X,'***SPEED GOES DOWN TO ZERO BEFORE LOAD TORQUE IS
        1IS REACHED***')
        STOP
```

```
      GO TO 201
180   IF(Z2INIT.GT.Z2FINA)GO TO 202
      Z2INIT=Z2INIT+E2
      GO TO  203
202   Z2INIT=Z2INIT-E2
      GO TO 203
190   IF(Z5INIT.GT.Z5FINA)GO TO 204
      Z5INIT=Z5INIT+E1
      GO TO 205
204   Z5INIT=Z5INIT-E1
      GO TO 205
      STOP
      END
C     ------------------------------------------------------------------
CCC   | MAIN PROGRAM ENDS                                              |
C     ------------------------------------------------------------------


C     ------------------------------------------------------------------
CCC   | CALCULATION OF FIRING AND EXTINCTION ANGLES DONE               |
C     ------------------------------------------------------------------

      SUBROUTINE ALBE(W,X,Y,K)
      DIMENSIONW(50),X(50)
      PI=3.1416
      DO 10 I=1,K
      W(I)=(2.*I-1.-Y)*PI/(2.*K)
      X(I)=(2.*I-1.+Y)*PI/(2.*K)
10    CONTINUE
      RETURN
      END
C     ------------------------------------------------------------------
CCC   | FINDS THE D.C.VOLTAGE RATIO ASSUMING CONTINOUS CONDUCTION      |
C     ------------------------------------------------------------------

      SUBROUTINE RATIO(W,X,K,Y)
      DIMENSION W(50),X(50)
      AR=0.0
      DO 10 I=1,K
      AR=AR+COS(W(I))+(-1.)*(COS(X(I)))
10    CONTINUE
      Y=AR/2.
      RETURN
      END
C     ------------------------------------------------------------------
CCC   | FINDS THE GATE FIRING VARIABLE AT PARTICULAR TIME              |
C     ------------------------------------------------------------------

      SUBROUTINE MODE(X,Y,Z,U,N)
      DIMENSION Y(5)
      PI=3.1416
      THETA=X*2.*PI*U
      A=PI/N
      IF(THETA.LE.A)GO TO 10
      IF(THETA.LE.(2.*A))GO TO 20
      IF(THETA.LE.(3.*A))GO TO 30
      IF(THETA.LE.(4.*A))GO TO 40
      AK=5.
      IF(THETA.GT.(4.*A+A/2.))GO TO 50
      GO TO 60
40    AK=4.
```

```
      IF(THETA.GT.(3.*A+A/2.))GO TO 50
      GO TO 60
30    AK=3.
      IF(THETA.GT.(2.*A+A/2.))GO TO 50
      GO TO 60
20    AK=2.
      IF(THETA.GT.(A+A/2.))GO TO 50
      GO TO 60
10    AK=1.
      IF(THETA.GT.(A/2.))GO TO 50
60    VC=((-1.)*(2.*N*THETA-PI*(2.*AK-1.)))/PI
      IF((ABS(Z)-ABS(VC)).GE.0.0)GO TO 70
90    Y(2)=1.;Y(1)=0.0
      Y(4)=1.;Y(3)=0.0
      GO TO 80
70    Y(1)=1.;Y(2)=0.0
      Y(4)=1.;Y(3)=0.0
      GO TO 80
50    VC=(2.*N*THETA-PI*(2.*AK-1.))/PI
      IF((ABS(Z)-ABS(VC)).GE.0.0)GO TO 70
      GO TO 90
80    CONTINUE
      RETURN
      END

C     ------------------------------------------------------------------
CC    | FINDS THE DIODE LOGIC VARIABLE                                 |
C     ------------------------------------------------------------------

      SUBROUTINE DIODE(X,Y,Z,I)
      DIMENSION X(5),Y(5,1000),Z(5)
      J=1
40    IF(X(J).GT.0.0)GO TO 10
      IF(Z(J).GT.0.0)GO TO 10
      Y(J,I)=0.0
      X(J)=0.0
      GO TO 20
10    Y(J,I)=1.
      Z(J)=0.0
20    J=J+1
      IF(J.GT.2)GO TO 30
      GO TO 40
30    RETURN
      END

C     ------------------------------------------------------------------
CC    | FINDS THE THYRISTOR LOGIC VARIABLE                             |
C     ------------------------------------------------------------------

      SUBROUTINE THYRIS
      COMMON/LOGIC/Y(5,1000),YY(5,1000),W(5,1000),JJ
      COMMON/CUR/X(5),XX(5),XXX(5)
      COMMON/VOL/Z(5),ZZ(5),ZZZ(5)
      COMMON/FIRING/U(5)
      J=1
      JJJ=JJ-1
60    IF(U(J).EQ.1.)GO TO 10
      IF(X(J).GT.0.0)GO TO 20
40    Y(J,JJ)=0.0
      X(J)=0.0
      GO TO 30
10    IF(X(J).GT.0.0)GO TO 20
      IF(Z(J).GT.0.0)GO TO 20
      GO TO 40
20    Y(J,JJ)=1.
```

```
      Z(J)=0.0
30    J=J+1
      IF(J.GT.4)GO TO 50
      GO TO 60
50    IF(Y(1,JJ).NE.1.)GO TO 70
      IF(Y(2,JJ).NE.1.)GO TO 70
      IF(Y(1,JJJ).EQ.1.)GO TO 80
      Y(2,JJ)=0.0
      X(2)=0.0
      W(2,JJ)=1.0
      GO TO 70
80    Y(1,JJ)=0.0
      X(1)=0.0
      W(1,JJ)=1.0
70    RETURN
      END
C     ------------------------------------------------------------------
CCC   | FINDS VALUE OF STATE VARIABLE Z1                                |
C     ------------------------------------------------------------------
      SUBROUTINE LOOP21
      COMMON/LOGIC/W(5,1000),TT(5,1000),T(5,1000),J
      COMMON/DROP/V,U
      COMMON/LOOP1/X,S,Z
      COMMON/STATE1/Y(1000)
      COMMON/STEP/A
      COMMON/CUR/BB(5),BBB(5),B(5)
      JJ=J-1
      IF(T(1,J).EQ.0.0)GO TO 10
      IF(W(2,J).EQ.0.0)GO TO 10
      X=S+((Y(JJ)-U-V)/Z)*A
      IF(X.LT.0.0)GO TO 20
      GO TO 10
20    X=0.0
      T(1,J)=0.0
      B(1)=0.0
10    RETURN
      END
C     ------------------------------------------------------------------
CCC   | FINDS THE VALUE OF STATE VARIABLE Z2                            |
C     ------------------------------------------------------------------
      SUBROUTINE LOOP12
      COMMON/LOGIC/W(5,1000),WW(5,1000),T(5,1000),J
      COMMON/DROP/V,U
      COMMON/LOOP2/X,S,Z
      COMMON/STATE1/Y(1000)
      COMMON/STEP/A
      COMMON/CUR/BB(5),BBB(5),B(5)
      JJ=J-1
      IF(T(2,J).EQ.0.0)GO TO 10
      IF(W(1,J).EQ.0.0)GO TO 10
      X=S+(((-1.)*(Y(JJ)+U+V))/Z)*A
      IF(X.LT.0.0)GO TO 20
      GO TO 10
20    X=0.0
      T(2,J)=0.0
      B(2)=0.0
10    RETURN
      END
C     ------------------------------------------------------------------
C     | FINDS THE VALUE OF STATE VARIABLE Z4                            |
```

```
C     ------------------------------------------------------------------
      SUBROUTINE CAPVOL
      COMMON/CAP/X,S,V
      COMMON/STATE/Y(1000),U(1000),Z(1000),Q(1000)
      COMMON/LOGIC/W(5,1000),T(5,1000),D(5,1000),J
      COMMON/STEP/AA
      COMMON/CUR/PPP(5),P(5),PP(5)
      JJ=J-1
      IF(T(1,J).NE.1.0)GO TO 10
      IF(T(2,J).NE.1.0)GO TO 10
      IF(W(2,J).EQ.1.)GO TO 20
      P(2)=Z(J)-Q(JJ)
      X=S+((P(2)+U(J))/V)*AA
      GO TO 30
20    P(1)=Q(JJ)
      X=S+(((-1.)*(P(1)+Y(J)))/V)*AA
      GO TO 30
10    IF(W(2,J).EQ.1.)GO TO 50
      A=(W(4,J)*W(1,J)*T(2,J)*Z(J)+U(J)*D(2,J))/V
      B=0.0
      GO TO 40
50    A=0.0
      B=(-1.)*(W(4,J)*T(1,J)*Z(J)+Y(J)*D(1,J))/V
40    X=S+(A+B)*AA
30    RETURN
      END

C     ------------------------------------------------------------------
CCC   | FINDS THE VOLTAGE ACROSS EACH ACTIVE DEVICE WHEN OUTPUT CURRENT |
CCC   | FALLS DOWN TO ZERO i.e.WHEN ALL DEVICES ARE OFF                 |
C     ------------------------------------------------------------------

      SUBROUTINE DISVOL
      COMMON/VOL/D(5),E(5),C(5)
      COMMON/TIME/A,X,Z,Y
      COMMON/CAPVO/B
      F=A/3.
      G=B/2.
      H=X*SIN(Y*Z)/2.
      D(1)=(-1.)*(F+G)
      D(2)=G-F
      D(3)=(-1.)*(F+H)
      D(4)=H-F
      E(1)=G-F-H
      E(2)=H-G-F
      C(1)=-D(1)
      C(2)=-D(2)
      RETURN
      END

C     ------------------------------------------------------------------
CCC   | FINDS THE VALUE OF STATE VARIABLE Z3                            |
C     ------------------------------------------------------------------

      SUBROUTINE OUTCUR
      COMMON/OCUR/V,D
      COMMON/DROP/R,S
      COMMON/LOGIC/C(5,1000),B(5,1000),BBB(5,1000),J
      COMMON/PAR/U,T,A
      COMMON/TIME/W,X,Y,E
      COMMON/STATE1/Z(1000)
      COMMON/STEP/CC
      JJ=J-1
      IF((B(1,J)-B(2,J)).EQ.0.0)GO TO 10
```

```
      F=X*SIN(E*Y)
      G=U*D
      H=2.*S
      IF(B(1,J).EQ.0.0)GO TO 20
      AA=(B(1,J)*C(4,J)*((F+Z(JJ)-G-W-R-H)*C(2,J)+(F-G-W-R-H)*C(1,J)))
     1/(A+T)
      BB=0.0
      GO TO 40
20    BB=((-1.)*B(2,J)*C(4,J)*((W+G+H+R)*C(2,J)+(W+G+H+R+Z(JJ))*C(1,J)
     1))/T
      AA=0.0
40    V=D+(AA+BB)*CC
      IF(V.GT.0.0)GO TO 30
      V=0.0
      GO TO 30
10    V=D
30    RETURN
      END

C     ------------------------------------------------------------
CC    | FINDS THE VALUE OF STATE VARIABLE Z5                     |
C     ------------------------------------------------------------

      SUBROUTINE INPCUR
      COMMON/TIME/R,Z,U,E
      COMMON/ICUR/X,D
      COMMON/LOGIC/B(5,1000),C(5,1000),BBB(5,1000),J
      COMMON/PAR/W,WW,Y
      COMMON/STEP/DD
      COMMON/STATE/PP(1000),PPP(1000),P(1000),PPPP(1000)
      COMMON/STATE1/Z4(1000)
      F=Z*SIN(U*E)
      IF(B(1,J).EQ.0.0)GO TO 10
      AA=(F/Y)*B(4,J)
      BB=0.0
      GO TO 20
10    BB=((F+Z4(J))*B(4,J))/Y
      AA=0.0
20    X=D+(AA+BB)*DD
      IF(X.GE.P(J))X=P(J)
      IF(X.LE.0.0)X=0.0
      RETURN
      END

C     ------------------------------------------------------------
CCC   | FINDS CURRENT ACROSS EACH CONDUCTING DEVICE WHEN BOTH D(1) AND |
CCC   | D(2) ARE CONDUCTING.                                     |
C     ------------------------------------------------------------

      SUBROUTINE BOTH
      COMMON/LOGIC/X(5,1000),Y(5,1000),Z(5,1000),J
      COMMON/CUR/D(5),E(5),C(5)
      COMMON/STATE/P(1000),U(1000),B(1000),W(1000)
      D(4)=B(J)
      E(1)=W(J)
      E(2)=B(J)-W(J)
      IF(Z(1,J).EQ.1.)C(1)=P(J)
      IF(Z(2,J).EQ.1.)C(2)=U(J)
      IF(X(1,J).EQ.1.)GO TO 10
      IF(X(2,J).EQ.1.)GO TO 20
10    IF(E(2).LE.0.0)GO TO 40
      GO TO 30
40    D(1)=B(J)+U(J)*Z(2,J)
      Y(2,J)=0.0
      E(2)=0.0
```

```
      GO TO 30
20    IF(E(1).LE.0.0)GO TO 50
      GO TO 30
50    D(2)=B(J)+P(J)*Z(1,J)
      Y(1,J)=0.0
      E(1)=0.0
30    RETURN
      END

C     ------------------------------------------------------------------
CC    | FINDS THE VOLTAGE ACROSS EACH DEVICE WHEN THEY ARE OFF          |
C     ------------------------------------------------------------------

      SUBROUTINE VOLTAG
      COMMON/LOGIC/X(5,1000),U(5,1000),Y(5,1000),J
      COMMON/VOL/S(5),T(5),D(5)
      COMMON/TIME/ZZ,Z,A,W
      COMMON/DROP/E,C
      COMMON/STATE1/B(1000)
      G=Z*SIN(A*W)
      IF(X(1,J).EQ.0.0)S(1)=(C-B(J))*X(2,J)
      IF(X(2,J).EQ.0.0)S(2)=(B(J)+C)*X(1,J)
      IF(X(3,J).EQ.0.0)S(3)=(C-G)*X(4,J)
      IF(X(4,J).EQ.0.0)S(4)=(C+G)*X(3,J)
      IF(Y(1,J).EQ.0.0)D(1)=(-1.)*S(1)
      IF(Y(2,J).EQ.0.0)D(2)=(-1.)*S(2)
      IF(U(1,J).EQ.0.0)T(1)=(B(J)+E+G)*U(2,J)
      IF(U(2,J).EQ.0.0)T(2)=(E-B(J)-G)*U(1,J)
      RETURN
      END

C     ------------------------------------------------------------------
CC    | FINDS THE CURRENT THROUGH EACH DEVICE WHEN THEY ARE ON          |
C     ------------------------------------------------------------------

      SUBROUTINE CURREN
      COMMON/LOGIC/X(5,1000),Y(5,1000),W(5,1000),J
      COMMON/CUR/E(5),F(5),D(5)
      COMMON/STATE/Z(1000),A(1000),B(1000),C(1000)
      IF(X(1,J).EQ.1.)E(1)=X(4,J)*(B(J)+A(J)*W(2,J))
      IF(X(2,J).EQ.1.)E(2)=X(4,J)*(B(J)+Z(J)*W(1,J))
      IF(X(4,J).EQ.1.)E(4)=B(J)
      IF(Y(1,J).EQ.1.)F(1)=B(J)
      IF(Y(2,J).EQ.1.)F(2)=B(J)
      IF(W(1,J).EQ.1.)D(1)=Z(J)
      IF(W(2,J).EQ.1.)D(2)=A(J)
      RETURN
      END

C     ------------------------------------------------------------------
CC    | FINDS THE OUTPUT VOLTAGE                                        |
C     ------------------------------------------------------------------

      SUBROUTINE OUTVOL
      COMMON/VOUT/OUT(1000)
      COMMON/STATE1/Z4(1000)
      COMMON/TIME/E,EM,T,W
      COMMON/LOGIC/X(5,1000),Y(5,1000),Z(5,1000),J
      F=EM*SIN(W*T)
      IF(X(1,J).NE.1.)GO TO 15
      IF(X(4,J).NE.1.)GO TO 20
      GO TO 10
15    IF(X(2,J).NE.1.)GO TO 20
      IF(X(4,J).NE.1.)GO TO 20
      IF(Y(2,J).EQ.1.)GO TO 30
```

```
      OUT(J)=(F+Z4(J))*Y(1,J)
      GO TO 20
30    OUT(J)=0.0
      GO TO 20
10    IF(Y(2,J).EQ.1.)GO TO 40
      OUT(J)=F*Y(1,J)
      GO TO 20
40    OUT(J)=-Z4(J)
20    RETURN
      END

C     ------------------------------------------------------------------
CC    | PRINTS THE STATEMENT FOR A PARTICULAR MODE                      |
C     ------------------------------------------------------------------

      SUBROUTINE PRIMOD(J)
      COMMON/LOGIC/SS(5,1000),DD(5,1000),DL(5,1000),M
      COMMON/FLAG/FL1,FL2,FL3,FL4,FL5,FL6,FL7,FL8,FL9,FL10,FL11,FL12
      IF(SS(1,J).NE.1.)GO TO 25
      IF(SS(4,J).EQ.1.)GO TO 15
      GO TO 200
25    IF(SS(2,J).NE.1.)GO TO 200
      IF(SS(4,J).EQ.1.)GO TO 40
      GO TO 200
15    IF(DD(1,J).EQ.1.)GO TO 20
      IF(DD(2,J).EQ.1.)GO TO 30
      GO TO 200
40    IF(DD(2,J).EQ.1.)GO TO 50
      IF(DD(1,J).EQ.1.)GO TO 60
      GO TO 200
20    IF(DD(2,J).EQ.1.)GO TO 70
      IF(DL(2,J).EQ.1.)GO TO 110
      GO TO 120
30    IF(DL(2,J).EQ.1.)GO TO 130
      GO TO 140
50    IF(DD(1,J).EQ.1.)GO TO 80
      IF(DL(1,J).EQ.1.)GO TO 170
      GO TO 180
60    IF(DL(1,J).EQ.1.)GO TO 190
      GO TO 210
70    IF(DL(2,J).EQ.1.)GO TO 90
      GO TO 100
80    IF(DL(1,J).EQ.1.)GO TO 150
      GO TO 160
19    FORMAT(/1X,130('-')/)
90    IF(FL1.EQ.1.)GO TO 200
      FL2=0.;FL3=0.;FL4=0.;FL5=0.;FL6=0.;FL7=0.;FL8=0.;FL9=0.;FL10=0.
      FL11=0.;FL12=0.
      FL1=1.
      PRINT 19
      PRINT 1
1     FORMAT(1X,'**  "NEW MODE BEGINS,THE ACTIVE DEVICES CONDUCTING
      1HERE ARE:S(1),S(4),D(1),D(2),DL(2)"  **')
      PRINT 19
      GO TO 200
100   IF(FL2.EQ.1.)GO TO 200
      FL1=0.;FL3=0.;FL4=0.;FL5=0.;FL6=0.;FL7=0.;FL8=0.;FL9=0.;FL10=0.
      FL11=0.;FL12=0.
      FL2=1.
      PRINT 19
      PRINT 2
2     FORMAT(1X,'**  "NEW MODE BEGINS,THE ACTIVE DEVICES CONDUCTING
      1HERE ARE:S(1),S(4),D(1),D(2)"  **')
      PRINT 19
      GO TO 200
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110     IF(FL3.EQ.1.)GO TO 200
        FL1=0.;FL2=0.;FL4=0.;FL5=0.;FL6=0.;FL7=0.;FL8=0.;FL9=0.;FL10=0.
        FL11=0.;FL12=0.
        FL3=1.
        PRINT 19
        PRINT 3
3       FORMAT(1X,'**  "NEW MODE BEGINS,THE ACTIVE DEVICES CONDUCTING
        1HERE ARE:S(1),S(4),D(1),DL(2)"  **')
        PRINT 19
        GO TO 200
120     IF(FL4.EQ.1.)GO TO 200
        FL1=0.;FL2=0.;FL3=0.;FL5=0.;FL6=0.;FL7=0.;FL8=0.;FL9=0.;FL10=0.
        FL11=0.;FL12=0.
        FL4=1.
        PRINT 19
        PRINT 4
4       FORMAT(1X,'**  "NEW MODE BEGINS,THE ACTIVE DEVICES CONDUCTING
        1HERE ARE:S(1),S(4),D(1)"  **')
        PRINT 19
        GO TO 200
130     IF(FL5.EQ.1.)GO TO 200
        FL1=0.;FL2=0.;FL3=0.;FL4=0.;FL6=0.;FL7=0.;FL8=0.;FL9=0.;FL10=0.
        FL11=0.;FL12=0.
        FL5=1.
        PRINT 19
        PRINT 5
5       FORMAT(1X,'**  "NEW MODE BEGINS,THE ACTIVE DEVICES CONDUCTING
        1HERE ARE:S(1),S(4),D(2),DL(2)"  **')
        PRINT 19
        GO TO 200
140     IF(FL6.EQ.1.)GO TO 200
        FL1=0.;FL2=0.;FL3=0.;FL4=0.;FL5=0.;FL7=0.;FL8=0.;FL9=0.;FL10=0.
        FL11=0.;FL12=0.
        FL6=1.
        PRINT 19
        GO TO 200
        PRINT 6
6       FORMAT(1X,'**  "NEW MODE BEGINS,THE ACTIVE DEVICES CONDUCTING
        1HERE ARE:S(1),S(4),D(2)"  **')
        PRINT 19
150     IF(FL7.EQ.1.)GO TO 200
        FL1=0.;FL2=0.;FL3=0.;FL4=0.;FL5=0.;FL6=0.;FL8=0.;FL9=0.;FL10=0.
        FL11=0.;FL12=0.
        FL7=1.
        PRINT 19
        PRINT 7
7       FORMAT(1X,'**  NEW MODE BEGINS,THE ACTIVE DEVICES CONDUCTING
        1HERE ARE:S(2),S(4),D(1),D(2),DL(1)"  **')
        PRINT 19
        GO TO 200
160     IF(FL8.EQ.1.)GO TO 200
        FL1=0.;FL2=0.;FL3=0.;FL4=0.;FL5=0.;FL6=0.;FL7=0.;FL9=0.;FL10=0.
        FL11=0.;FL12=0.
        FL8=1.
        PRINT 19
        PRINT 8
8       FORMAT(1X,'**  "NEW MODE BEGINS,THE ACTIVE DEVICES CONDUCTING
        1HERE ARE:S(2),S(4),D(1),D(2)"  **')
        PRINT 19
        GO TO 200
170     IF(FL9.EQ.1.)GO TO 200
        FL1=0.;FL2=0.;FL3=0.;FL4=0.;FL5=0.;FL6=0.;FL7=0.;FL8=0.;FL10=0.
        FL11=0.;FL12=0.
        FL9=1.
        PRINT 19
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```
      PRINT 9
9     FORMAT(1X,'**  "NEW MODE BEGINS,THE ACTIVE DEVICES CONDUCTING
     1HERE ARE:S(2),S(4),D(2),DL(1)"  **')
      PRINT 19
      GO TO 200
180   IF(FL10.EQ.1.)GO TO 200
      FL1=0.;FL2=0.;FL3=0.;FL4=0.;FL5=0.;FL6=0.;FL7=0.;FL8=0.;FL9=0.
      FL11=0.;FL12=0.
      FL10=1.
      PRINT 19
      PRINT 10
10    FORMAT(1X,'**  "NEW MODE BEGINS,THE ACTIVE DEVICES CONDUCTING
     1HERE ARE:S(2),S(4),D(2)"  **')
      PRINT 19
      GO TO 200
190   IF(FL11.EQ.1.)GO TO 200
      FL1=0.;FL2=0.;FL3=0.;FL4=0.;FL5=0.;FL6=0.;FL7=0.;FL8=0.;FL9=0.
      FL10=0.;FL12=0.
      FL11=1.
      PRINT 19
      PRINT 11
11    FORMAT(1X,'**  "NEW MODE BEGINS,THE ACTIVE DEVICES CONDUCTING
     1HERE ARE:S(2),S(4),D(1),DL(1)"  **')
      PRINT 19
      GO TO 200
210   IF(FL12.EQ.1.)GO TO 200
      FL1=0.;FL2=0.;FL3=0.;FL4=0.;FL5=0.;FL6=0.;FL7=0.;FL8=0.;FL9=0.
      FL10=0.;FL11=0.
      FL12=1.
      PRINT 19
      PRINT 12
12    FORMAT(1X,'**  "NEW MODE BEGINS,THE ACTIVE DEVICES CONDUCTING
     1HERE ARE:S(2),S(4),D(1)"  **')
      PRINT 19
200   RETURN
      END
C     ------------------------------------------------------------
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APEENDIX-II-B.

SAMPLE OUTPUT LISTING FOR SIMULATION PROGRAM FOR THE AC-DC CHOPPER FEEDING A SEPERATELY EXCITED DC MOTOR.THE LISTING IS ONLY FOR THE FIRST CHOP.

THE PASSIVE VALUES OF THE COMMUTATING ELEMENTS ARE:L1=L2=.000192H C=.000015F;INPUT SOURCE INDUCTANCE=.000390H;MOTOR BACK EMF. CONSTANT=1.378;THE EDDY CURRENT MODEL MOTOR PARAMETERS ARE: ARMATURE CIRCUIT RESISTANCE=2.192OHMS,FICTITIOUS SHUNTING RESISTANCE =4.60HMS,TOTAL ARMARTURE CIRCUIT INDUCTANCE=.0228H

S(2),S(4),D(2) CONDUCT INITIALLY.

INITIAL VALUES OF STATE VARIABLES ARE:Z1=0.0,Z2=0.0,Z3=10.1, Z4=-361.5,Z5=0.0

OUTPUT CURRENT= 9.756AMPS SPEED= 671.5RPM

ID1 (AMPS)	ID2 (AMPS)	Id (AMPS)	Vc (VOLTS)	I (AMPS)	Vd (VOLTS)	TIME (SECS)
0.00	0.00	9.18	-289.20	0.00	0.00	.000020
0.00	0.00	9.08	-289.20	0.00	0.00	.000040
0.00	0.00	8.97	-289.20	0.00	0.00	.000060
0.00	0.00	8.86	-289.20	0.00	0.00	.000080
0.00	0.00	8.76	-289.20	0.00	0.00	.000100
0.00	0.00	8.65	-289.20	0.00	0.00	.000120
0.00	0.00	8.54	-289.20	0.00	0.00	.000140
0.00	0.00	8.44	-289.20	0.00	0.00	.000160
0.00	0.00	8.33	-289.20	0.00	0.00	.000180
0.00	0.00	8.23	-289.20	0.00	0.00	.000200
0.00	0.00	8.12	-289.20	0.00	0.00	.000220
0.00	0.00	8.01	-289.20	0.00	0.00	.000240
0.00	0.00	7.91	-289.20	0.00	0.00	.000260
0.00	0.00	7.80	-289.20	0.00	0.00	.000280
0.00	0.00	7.70	-289.20	0.00	0.00	.000300
0.00	0.00	7.60	-289.20	0.00	0.00	.000320
0.00	0.00	7.49	-289.20	0.00	0.00	.000340
0.00	0.00	7.39	-289.20	0.00	0.00	.000360
0.00	0.00	7.28	-289.20	0.00	0.00	.000380
0.00	0.00	7.18	-289.20	0.00	0.00	.000400
0.00	0.00	7.08	-289.20	0.00	0.00	.000420
0.00	0.00	6.97	-289.20	0.00	0.00	.000440
0.00	0.00	6.87	-289.20	0.00	0.00	.000460
0.00	0.00	6.77	-289.20	0.00	0.00	.000480
0.00	0.00	6.67	-289.20	0.00	0.00	.000500
0.00	0.00	6.56	-289.20	0.00	0.00	.000520

MODE CHANGE:S(1),S(4),D(2),DL(2) ARE CONDUCTING

0.00	8.97	6.61	-282.97	0.00	282.97	.000526
0.00	17.75	6.65	-273.21	0.00	273.21	.000532
0.00	26.22	6.70	-260.04	0.00	260.04	.000538
0.00	34.28	6.73	-243.63	0.00	243.63	.000544
0.00	41.83	6.77	-224.19	0.00	224.19	.000550
0.00	48.77	6.80	-201.97	0.00	201.97	.000556
0.00	55.02	6.82	-177.23	0.00	177.23	.000562
0.00	60.49	6.84	-150.30	0.00	150.30	.000568
0.00	65.12	6.84	-121.52	0.00	121.52	.000574
0.00	68.85	6.85	-91.24	0.00	91.24	.000580
0.00	71.64	6.84	-59.85	0.00	59.85	.000586
0.00	73.44	6.82	-27.74	0.00	27.74	.000592

MODE CHANGE:S(1),S(4),D(1),D(2),DL(2) ARE CONDUCTING

0.00	74.24	6.82	4.68	0.88	-4.68	.000598
0.00	74.03	6.82	36.67	1.77	-36.67	.000604
0.00	72.82	6.82	67.82	2.67	-67.82	.000610
0.00	70.63	6.82	97.74	3.58	-97.74	.000616
0.00	67.51	6.82	126.04	4.50	-126.04	.000622
0.00	63.51	6.82	152.38	5.42	-152.38	.000628
0.00	58.68	6.82	176.41	6.36	-176.41	.000634

MODE CHANGE:S(1),S(4),D(1),DL(2) ARE CONDUCTING

0.00	53.10	6.82	197.84	6.82	61.34	.000640
0.00	46.86	6.81	216.58	6.81	61.91	.000646
0.00	40.02	6.80	232.59	6.80	62.48	.000652
0.00	32.69	6.78	245.66	6.78	63.05	.000658
0.00	24.95	6.77	255.64	6.77	63.63	.000664
0.00	16.89	6.75	262.40	6.75	64.20	.000670
0.00	8.63	6.74	265.85	6.74	64.77	.000676
0.00	0.25	6.73	265.95	6.73	65.34	.000682

MODE CHANGE:S(1),S(4),D(1) ARE CONDUCTING.

0.00	0.00	6.72	265.95	6.72	65.91	.000688
0.00	0.00	6.67	265.95	6.67	66.48	.000708
0.00	0.00	6.63	265.95	6.63	68.38	.000728
0.00	0.00	6.59	265.95	6.59	70.28	.000748
0.00	0.00	6.55	265.95	6.55	72.18	.000768
0.00	0.00	6.52	265.95	6.52	74.07	.000788
0.00	0.00	6.48	265.95	6.48	75.96	.000808
0.00	0.00	6.45	265.95	6.45	77.85	.000828
0.00	0.00	6.42	265.95	6.42	79.73	.000848
0.00	0.00	6.39	265.95	6.39	81.61	.000868
0.00	0.00	6.36	265.95	6.36	83.49	.000888
0.00	0.00	6.34	265.95	6.34	85.36	.000908
0.00	0.00	6.31	265.95	6.31	87.24	.000928
0.00	0.00	6.29	265.95	6.29	89.10	.000948
0.00	0.00	6.27	265.95	6.27	90.97	.000968
0.00	0.00	6.25	265.95	6.25	92.83	.000988
0.00	0.00	6.23	265.95	6.23	94.68	.001008
0.00	0.00	6.22	265.95	6.22	96.54	.001028
0.00	0.00	6.20	265.95	6.20	98.39	.001048
0.00	0.00	6.19	265.95	6.19	100.23	.001068
0.00	0.00	6.18	265.95	6.18	102.07	.001088
0.00	0.00	6.17	265.95	6.17	103.91	.001108
0.00	0.00	6.16	265.95	6.16	105.74	.001128
0.00	0.00	6.16	265.95	6.16	107.57	.001148
0.00	0.00	6.15	265.95	6.15	109.40	.001168
0.00	0.00	6.15	265.95	6.15	111.22	.001188
0.00	0.00	6.15	265.95	6.15	113.03	.001208
0.00	0.00	6.15	265.95	6.15	114.84	.001228
0.00	0.00	6.15	265.95	6.15	116.65	.001248
0.00	0.00	6.15	265.95	6.15	118.45	.001268
0.00	0.00	6.16	265.95	6.16	120.25	.001288
0.00	0.00	6.16	265.95	6.16	122.04	.001308
0.00	0.00	6.17	265.95	6.17	123.83	.001328
0.00	0.00	6.18	265.95	6.18	125.61	.001348
0.00	0.00	6.19	265.95	6.19	127.39	.001368
0.00	0.00	6.20	265.95	6.20	129.17	.001388
0.00	0.00	6.22	265.95	6.22	130.93	.001408
0.00	0.00	6.23	265.95	6.23	132.70	.001428
0.00	0.00	6.25	265.95	6.25	134.45	.001448
0.00	0.00	6.27	265.95	6.27	136.21	.001468
0.00	0.00	6.29	265.95	6.29	137.95	.001488

0.00	0.00	6.31	265.95	6.31	139.70	.001508
MODE CHANGE:S(2),S(4),D(1),DL(1) ARE CONDUCTING.						
8.25	0.00	6.39	260.10	6.39	401.53	.001514
16.31	0.00	6.46	250.99	6.46	392.94	.001520
24.09	0.00	6.53	238.74	6.53	381.21	.001526
31.48	0.00	6.60	223.51	6.60	366.50	.001532
38.40	0.00	6.67	205.48	6.67	348.99	.001538
44.76	0.00	6.73	184.89	6.73	328.91	.001544
50.47	0.00	6.79	161.99	6.79	306.53	.001550
55.46	0.00	6.84	137.07	6.84	282.13	.001556
59.68	0.00	6.88	110.44	6.88	256.02	.001562
63.07	0.00	6.91	82.45	6.91	228.54	.001568
65.58	0.00	6.94	53.44	6.94	200.05	.001574
67.18	0.00	6.97	23.78	6.97	170.90	.001580
67.86	0.00	6.98	-6.16	6.98	141.48	.001586
67.60	0.00	6.99	-35.99	6.99	112.16	.001592
66.41	0.00	6.99	-65.35	6.99	83.31	.001598
64.30	0.00	6.98	-93.86	6.98	55.31	.001604
61.31	0.00	6.96	-121.17	6.96	28.52	.001610
57.45	0.00	6.94	-146.93	6.94	3.27	.001616
52.80	0.00	6.91	-170.81	6.91	-20.10	.001622
MODE CHANGE:S(2),S(4),D(1),D(2),DL(1) ARE CONDUCTING.						
47.39	0.00	6.91	-192.53	6.27	0.00	.001628
41.31	0.00	6.91	-211.56	5.35	0.00	.001634
34.63	0.00	6.91	-227.56	4.19	0.00	.001640
27.46	0.00	6.91	-240.22	2.85	0.00	.001646
19.88	0.00	6.91	-249.31	1.37	0.00	.001652
MODE CHANGE:S(2),S(4),D(2),DL(1) ARE CONDUCTING.						
12.03	0.00	6.91	-254.67	0.00	0.00	.001658
4.00	0.00	6.88	-256.27	0.00	0.00	.001664
MODE CHANGE:S(2),S(4),D(2) ARE CONDUCTING.						
0.00	0.00	6.85	-256.27	0.00	0.00	.001670
0.00	0.00	6.75	-256.27	0.00	0.00	.001690
0.00	0.00	6.64	-256.27	0.00	0.00	.001710
0.00	0.00	6.54	-256.27	0.00	0.00	.001730
0.00	0.00	6.44	-256.27	0.00	0.00	.001750
0.00	0.00	6.34	-256.27	0.00	0.00	.001770
0.00	0.00	6.24	-256.27	0.00	0.00	.001790